SERVICE MANUAL

NELLCOR® N-200 PULSE OXIMETER

NOTICE:

This manual is provided for the purpose of servicing the *NELLCOR* N-200 pulse oximeter. It is provided without charge by Nellcor Incorporated. This manual contains unpublished proprietary information and is not to be copied, transmitted, or used for any other purpose. Additional copies are available upon request by writing the Company at the address below.

Caution: Federal law (U.S.) restricts this device to sale by or on the order of a physician.

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WARNING: The *NELLCOR* N-200 pulse oximeter contains no user-servicable parts. For protection against electrical hazard, refer all servicing to qualified personnel.

WARNING: For continued protection against fire hazard, replace fuses only with the same type and rating.

WARNING: The *NELLCOR* N-200 pulse oximeter is a patient-connected medical device. An isolated patient connector is provided to protect the patient from potentially dangerous electrical potentials or ground paths. To protect the integrity of this connection, the procedures and part specifications contained in this manual must be adhered to.

SECTION 1

INTRODUCTION

This manual covers test and repair of the *NELLCOR*® N-200 pulse oximeter. The N-200 is identified by its two-piece construction. The front part of the N-200 is the monitor; the back part of the N-200 is the powerbase. The monitor receives, processes, and stores patient pulse data; the powerbase provides AC power to the monitor and drives peripheral display and recording devices. Communication between monitor and powerbase is provided by a bi-directional optical link.

This manual is provided to qualified service personnel for the purpose of maintaining and repairing the *NELLCOR* N-200 pulse oximeter. Dangerous voltages are exposed when the cover is removed, certain components are critical to maintain patient isolation, and improper repair procedures can adversely affect the instrument's calibration. For the protection of service personnel and patients, the procedures described in this manual are only to be performed by qualified service personnel.

Repair and testing of the instrument exposes service personnel to potentially hazardous voltages, and improper repair or adjustment may affect the accuracy or patient protection associated with the instrument. Where appropriate, warnings or cautions have been included in the text of this manual. The term **"WARNING"** is used to bring attention to a procedure or precaution that is important to ensure the safety of the service personnel or possibly the patient. The word **"CAUTION"** brings attention to a procedure that should be carefully followed in order to prevent damage to the instrument or an error in calibration or performance. It is important that these warnings and cautions be read carefully and followed.

SECTION 2

DESCRIPTION OF THE INSTRUMENT

The *NELLCOR* N-200 pulse oximeter is intended for continuously monitoring arterial oxygen saturation and pulse rate. The measurement is made noninvasively by applying a reusable clip-on or disposable adhesive-attached sensor to a finger or other site on the patient to be monitored.

The instrument is a portable unit, weighing about 8 pounds total, with a self-contained battery intended for operation for periods of up to 2 hours during power failures or transport. The battery is recharged whenever the unit is connected to AC power, and is fully recharged in 14 hours.

Front panel controls allow adjustment of the beeper volume, alarm volumes, alarm disabling, and adjustment of alarm limits for high and low oxygen saturation, and high and low pulse rate. A connector is located on the front panel for connection of the patient module assembly. The standard patient cable is 4 meters in length and is terminated by a module containing a preamplifier and sensor and ECG connectors. The entire patient module assembly is isolated from ground with a maximum leakage current of 10 microamperes. This provides safety for the patient from currents generated by faulty equipment, e.g., defibrillators or electrosurgical units.

WARNING: To assure continued patient safety, the patient module or sensors must not be replaced with any parts other than those designated or manufactured by Nellcor Incorporated.

A number of patient safety and labor-saving features are incorporated into the N-200:

- *C-LOCK*™ ECG synchronization enhances performance in high-motion environments, such as the ICU or the NICU.
- Three operating modes provide different averaging times, adapting the N-200 for use in the presence of varying levels of patient activity.
- The N-200 is equipped with two sets of default alarm limits, one for use in monitoring adults and one for neonates.
- Twelve hours of oxygen saturation and pulse rate data are stored in the trend memory, and one hour of saturation, pulse rate, and pulse perfusion data are stored in the event memory. These data can be provided to a variety of analog or digital output devices.
- Noninvasive *NELLCOR* sensors obtain measurements by optical means alone, using two light-emitting diodes as light sources. Specific sensors are available for use on neonates, infants, children, and adults.
- Patented automatic calibration mechanisms are incorporated in the N-200 (U.S. Patent 4,621,643 and others pending). The N-200 automatically calibrates itself each time it is turned on, at periodic intervals thereafter, and whenever a new sensor is connected. Instrument sensitivity changes automatically to accommodate a wide range of tissue thicknesses and skin pigmentations.

Internally, the monitor contains five printed circuit boards (PCBs), the battery, and a speaker. The largest circuit board (mounted on the top cover of the monitor) is the processor PCB, which contains the analog processing circuitry and the microprocessor with its associated circuitry. The power supply PCB is located on the back of the monitor. The battery charger PCB is located along the left side of the instrument chassis when viewed from the front. The display and driver PCBs are located immediately behind the front panel and contain the LED displays and front-panel switches.

The powerbase contains a power supply transformer, a mother PCB and three daughter PCBs. The mother PCB is mounted vertically at the front of the powerbase (facing the monitor); the daughter PCBs are mounted horizontally and mate to the mother PCB. Details of instrument assembly and disassembly are found in Section 4.

SECTION 3

THEORY OF OPERATION

Theory of operation is presented in two parts. First, a general overview of the N-200's capabilities and the physical principles of its operation is presented. Next, the details of circuit operation are discussed.

3.1. GENERAL THEORY

The *NELLCOR* N-200 provides continuous, noninvasive, self-calibrated measurements of both functional oxygen saturation and pulse rate.

The instrument combines the principles of spectrophotometric oximetry and plethysmography. It consists of an electro-optical sensor that is applied to the patient and a microprocessor-based monitor that processes and displays the measurements. The electro-optical sensor contains two low-voltage, low-intensity light-emitting diodes (LEDs) as light sources and one photodiode as a light receiver. One LED emits red light (approximately 660 nm) and the other emits infrared light (approximately 920 nm).

When the light from the LEDs is transmitted through the tissue at the sensor site, a portion of the light is absorbed by skin, tissue, bone, and blood. The photodiode in the sensor measures the light that passes through, and this information is used to determine how much light was absorbed. The amount of absorption remains essentially constant during the diastolic (nonpulsatile) phase and is analogous to the reference measurement of a spectrophotometer.

With each heart beat, a pulse of oxygenated arterial blood flows to the sensor site. This oxygenated hemoglobin differs from deoxygenated hemoglobin in the amount of red and infrared light that it absorbs. The N-200 continuously measures absorption of both red and infrared light and uses those measurements to determine the percentage of functional hemoglobin that is saturated with oxygen.

When the pulsatile blood is present, the light absorption at both wavelengths is changed by the presence of that blood. The *NELLCOR* N-200 then corrects the measurements during the pulsatile flow for the amount of light absorbed at the initial measurements. The ratio of the corrected absorption at each wavelength is then used to calculate functional oxygen saturation.

3.1.1. *C-LOCK* ECG Synchronization

When the N-200 is provided with ECG input, it is receiving two signals that independently reflect cardiac activity: one from the sensor and the other from the ECG. This enhances the performance of the instrument in the presence of patient movement, as discussed below.

There is a time delay between the electrical and mechanical activity of the heart. When an ECG QRS-complex is detected, a pulse will be detected at the sensor site a short time later. The length of this delay varies with the heart rate, the patient's physiology, and the location of the sensor. The N-200 measures this time delay, and, after a few pulse beats, calculates the average delay between the occurrence of the R-wave and the detection of the optical pulse by the sensor. This average delay is used to establish a "time window" during which the optical pulse is expected at the sensor site.

A pulse that is received within this time window is considered a real pulse and is processed. A pulse that is received outside the time window is considered an artifact and is rejected. Both the average delay and the time window are recalculated with each pulse beat to adjust for changes in the patient's physiology. If the ECG signal is irregular or noisy, then the optical pulse alone is used to determine pulse rate and initiate saturation calculations. Since artifacts often appear independently in the ECG and pulse signals, this method provides the most stable measurement of pulse rate and saturation.

If either the optical pulse or the ECG signal is markedly degraded or lost, the appropriate alarm activates and *C-LOCK* ECG synchronization is suspended. It will resume once both inputs have been re-established.

3.1.2. Automatic Calibration

Patented automatic calibration mechanisms are incorporated into the N-200 pulse oximetry system (U.S. Patent 4,621,643 and others pending). Each sensor is calibrated when it is manufactured: the effective mean wavelength of the red LED is determined, coded into a calibration resistor, and then checked. That calibration resistor is read by the N-200 software to determine the calibration coefficients that are used for the measurements obtained by that sensor.

The N-200 is automatically calibrated each time it is turned on, at periodic intervals thereafter, and when a new sensor is connected. Also, the intensity of each LED in the sensor is adjusted automatically to compensate for differences in tissue thickness.

3.1.3. Functional vs. Fractional Saturation

Because the N-200 measures functional oxygen saturation, it may produce measurements that differ from those of instruments that measure fractional oxygen saturation.

Functional oxygen saturation is defined as oxygenated hemoglobin expressed as a percentage of the hemoglobin that is capable of transporting oxygen. Because the N-200 uses two wavelengths to measure saturation, it measures only oxygenated and deoxygenated (i.e., functional) hemoglobin. It does not detect the presence of significant amounts of dysfunctional hemoglobin, such as carboxyhemoglobin or methemoglobin.

In contrast, some other laboratory instruments, such as the IL-282 CO-Oximeter, report fractional oxygen saturation values. Fractional saturation is defined as oxygenated hemoglobin expressed as a percentage of total hemoglobin, whether or not that hemoglobin is available for oxygen transport. Dysfunctional hemoglobin species are included in this calculation. Consequently, when measurements from the N-200 are compared with those from another instrument, it is important to consider whether the other instrument is measuring functional or fractional saturation.

3.1.4. Measured vs. Calculated Saturation

When oxygen saturation is calculated from blood gas PaO2, the calculated value may differ from the oxygen saturation measurement of the N-200. This is because an oxygen saturation value that has been calculated from blood gas PaO2 has not necessarily been correctly adjusted for the effect of variables that shift the relationship between PaO2 and saturation. These variables include temperature, pH, PaCO2, 2,3-DPG, and the concentration of fetal hemoglobin. Refer to the Operator's Manual for additional information.

3.2. CIRCUIT-LEVEL DESCRIPTION

Refer to Section 9 for the instrument schematic and block diagrams. The major circuit sections consist of:

- the patient module
- the analog processing circuitry and microprocessor circuitry
- the front panel display logic
- the battery charger and power supply
- the instrument powerbase, which contains the data communications interface circuitry.

Since the measurement of oxygen saturation requires light of two different wavelengths, two LEDs (one IR and one red) are used to generate light, which is passed through the tissue at the sensor site into a single photodiode. The LEDs are illuminated alternately with a four-state clock. The photodiode signal, representing light from both LEDs in sequence, is amplified and then separated by a two-channel synchronous detector, one channel sensitive to the infrared light waveform and the other sensitive to the red light waveform. These signals are then filtered to remove the LED switching frequency as well as electrical or ambient noise, and then digitized by an analog to digital (A:D) converter. This digital signal is then processed by the microprocessor to identify individual pulses and compute the oxygen saturation from the ratio of the pulse seen by the red wavelength compared to the pulse seen by the IR wavelength.

Throughout this section and on the schematics, active low logic signals are designated by an overbar above the signal name (for example, "SIGNAL").

3.3. PATIENT MODULE

The patient module contains preamplifiers for the saturation (SAT) and electrocardiogram (ECG) signals (refer to SCHEMATIC PATIENT MODULE PCB). Power for the circuitry is ± 15 V generated by the processor board.

The drive current for the pair of sensor LEDs is supplied from the instrument, generated on the processor board (VIR and VRED on SCHEMATIC PROCESSOR PCB, SHEET 4). This waveform is a bipolar current drive which is passed through the patient module to the back-to-back sensor LEDs. A positive current pulse drives the IR LED and a negative current pulse drives the red LED. The drive current is controlled by a feedback loop on the processor board in response to photodetector response.

The detector photodiode generates a current proportional to the amount of light received. SAT preamplifier U2 is a current to voltage (I:V) converter in an inverting configuration that converts the DETECTOR current to a SAT voltage signal. The conversion ratio is 250 mV/µA. Voltage regulator VR1 biases the preamplifier to approximately +8.5 V output for 0 current input. This bias increases the swing of the I:V converter to an effective output swing of +8.5 V to -10 V. The additional voltage headroom is necessary for high ambient light conditions.

Instrumentation amplifier U1 preamplifies the ECG signal. Gain of the amplifier is set for approximately 30. Neon lamps DS1, DS2, and DS3 are used to protect U1 from potentially damaging high-energy pulses which may result from defibrillation procedures. Series resistors R1 and R2 provide further isolation from high transient currents. Diodes CR1 through CR4 shunt high-voltage transients to the low-impedance power supplies. Resistors R3 and R4 pull the input signal lines to the power supply voltage levels when an ECG signal lead has become detached.

Common mode signals A1 and A2 from U1 are summed through R9 and R10, amplified, and inverted through operational amplifier U2. The output of U2 is fed back to the patient to maintain the patient at a constant potential and eliminate common mode signals from the input sensing leads. The ECG signal from U1 goes directly to the processor board.

The sensor contains a calibration resistor that codes the wavelength of the red LED mounted in the sensor. Because the wavelength of the red LED varies from one sensor to another, an error would result in the computation for oxygen saturation if not corrected for by the calibration resistor. This calibration resistor is connected directly through the instrument cable assembly to the processor board. Since the patient module assembly is used close to the patient environment, it is potted in epoxy to prevent any damage from moisture and is not repairable. In the event of failure or damage to the sensor contacts or to the cable or connector itself, the entire assembly must be replaced.

3.4. PROCESSOR PCB

The processor PCB contains most of the active circuitry in the N- 200, both analog and digital. Refer to SCHEMATIC PROCESSOR PCB, SHEETS 1 through 4, in the following discussion.

3.4.1. Digital Section

The digital section of the N-200 processor PCB is shown on SCHEMATIC PROCESSOR PCB, SHEET 1.

3.4.1.1. Microprocessor Subsection

The processing power of the N-200 pulse oximeter is contained within a standard 8088 minimum-mode microprocessor RAM/ROM configuration. Program memory is contained in one 64K x 8 EPROM (U21) while the 32K x 8 system RAM (U15) provides a data buffer, stack, scratchpad, and trend and event data memory functions. The RAM is mated to a clock/calendar socket, which provides time and date information used during trend and event recording, as well as battery back-up to prevent data loss when the instrument is in standby.

Processor (U8) pins 9 through 16, designated AD0-AD7, are multiplexed to alternately present the low-order address byte and a data byte. On the first clock cycle of an instruction, an address is present on these lines. The ALE signal (U8, pin 25) pulses high to latch the lower byte of the address in transparent octal latch U33. In the following clock cycles, data can flow bidirectionally on these lines.

The upper 4 address lines of U8 (A16 through A19) are also multiplexed, alternately carrying address and status information. Only the uppermost bit (A19) is used in the N-200 for address decoding. This pin (U8, pin 35) is at logic high when the system is addressing ROM space, and low when it is addressing RAM or performing input/output (I/O) functions. The processor's ALE signal latches this bit in flip-flop U3.

3.4.1.2. Memory Map

The entire processor system is memory mapped. That is, all devices on the 8088 data bus are accessed (read from or written to) at specific memory locations in the 1 Mbyte memory range. The upper 512 kbytes of memory are considered ROM space; the lower 512 kbytes are considered RAM and I/O space. ROM resides in the top 64 kbytes of memory, with the program starting at hex FFFF0 after reset. Since only 64 kbytes of the ROM space are actually used, images of the 64 kbyte ROM are repeated up to the 512 kbyte limit because memory is not uniquely decoded.

RAM begins at address 0 and extends for 32 kbytes. I/O functions reside directly above RAM, starting at address hex 8000. The I/O select lines coming from U17 and U23 are 16 addresses apart, ranging from hex 8000 to hex 80F0.

3.4.1.3. Wait State Generator

Two D-type flip-flops in U1 form a wait-state generator. A wait state of one clock cycle is generated whenever I/O is addressed (that is, whenever a peripheral device is accessed). Accessing RAM (addresses between 0 and 32k) generates no wait state.

3.4.1.4. Clock Generator

U2 produces a processor clock with the correct duty cycle, as well as a peripheral clock which drives UART U16 and the two timer chips U34 and U38. Because the 8088 processor U8 requires a 33% duty cycle clock, the crystal oscillator runs at 22.1184 MHz, three times the desired frequency. U2 divides the 22.1184 MHz signal by three and provides the correct duty cycle to U8.

A reset circuit composed of R1, CR1, and C19 ensure that U2, pin 11, is held low immediately following power-up. This maintains the logic at a known state while the power supplies and crystal oscillator stabilize.

3.4.1.5. Timer Circuits and UART

Additional peripheral devices include two 82C53 triple counter/timer chips U34 and U38 and UART device U16. The 82C53 sections control:

1. Display update interrupts to the 8088 at a 2.5 ms rate (also provides for real time references within the system program).

2. Baud rate for the 8251 UART (U16), which drives an optical data link for communication between the monitor and powerbase. The baud rate is set at 19.2 kbaud.

3. Audio frequency generation for the alarm beeper (TONE).

4. Clock frequency for the ECG switched-capacitor notch filter (NCLK).

5. Pattern generator clock frequency (the pattern generator is composed of U39, U35, and U28), which controls synchronous circuit operations.

3.4.1.6. Pattern Generator

The pattern generator (U39, U35, and U28) provides software selectable timing patterns used to control sync detector gating, LED control, and power supply synchronization triggers.

In operation, a preprogrammed bit pattern in EPROM U35 is continuously cycled through by counter U39, clocked by the divided down processor clock output. One of eight patterns can be selected through address lines A8-A10 on U35 through octal latch U40. Additional latch U28 serves to "de-glitch" the EPROM outputs by holding the last output byte while the counter steps to the next address. Various patterns within the EPROM are used to select LED/sync detector sampling speeds along with real time calibration patterns and diagnostic timing.

3.4.2. Analog Front End and LED Current Drive

The analog circuitry and LED drive circuitry is shown on SCHEMATIC PROCESSOR PCB SHEET 2.

3.4.2.1. Main Analog Signal Flow

The SAT signal from the patient module passes through a 50 kHz low-pass filter (one quarter of quad operational amplifier U27 in a 2-pole Butterworth configuration). The signal is then AC coupled to another U27 op amp, configured as a gain stage with unity gain. A variable attenuator composed of Digital-to-Analog Converter (DAC) U44 and amplifier U32 is followed by a noninverting amplifier (U32) with gain of 51. Together, the two circuits provide a programmable variable-gain function that can vary between 0 and 51. This gain is called INAMP (input amplifier) gain. In operation, the composite signal is always maximized by the operating software such that the largest possible signal is fed into the next stage of synchronous demodulation; this helps optimize the signal/noise (S/N) ratio.

Voltage regulator VR3 provides a low-noise 5 V DC supply for U44.

3.4.2.2. Sync Detector

The INAMP stage drives sync detector U32. If the $\overline{\text{SATINVERT}}$ signal is at logic low, U32, pin 10, is pulled to ground potential, and the stage becomes an inverting amplifier with unity gain. When $\overline{\text{SATINVERT}}$ is high, the stage becomes a noninverting voltage follower. Trimpot R123 is used to equalize the magnitudes of the inverting and noninverting gains.

3.4.2.3. Demultiplexer

The output of the sync detector drives both halves of U14. U14 demultiplexes the signal synchronously with the IRGATE and REDGATE steering pulses. Low-pass filters (R47 and C14; R52 and C30) suppress switching transients. The signal in each channel is then buffered by a unity-gain amplifier and low-pass filtered by two active-filter stages (each with two poles at approximately 20 Hz). The filters are slightly overdamped to improve step response.

The last stage in each channel is an offset amplifier with gain, which offsets the signals by a small positive voltage (approximately 0.25 V). This voltage is derived from VREF (set at 10 V) and the voltage dividers R50 and R46 (R80 and R74). Since the Analog-to-Digital Converter can only process 0 to 10 V signals, the positive bias provides a reference floor for analog-to-digital conversion stages that follow to ensure that the total chain offset errors of the op amps can never drive the outputs negative. Because the RED channel has twice the gain of the IR channel, the offset seen at TP10 is twice that seen at TP9 when no signal input is present.

3.4.2.4. Logic Flags

Several flags are produced in the analog section of the processor PCB that instruct the processor to vary circuit parameters (gain and LED drive currents) so that signal levels are kept safely below those which would saturate on-board electronics.

LEDHI — The SAT signal coming from the patient module can range from +8.5 V to -10 V without saturating the patient module's analog amplifiers. Comparator U20 compares the filtered (and halved) SAT signal to a -5 V reference. When the signal drops too low (SAT less than -10 V), the signal is too close to the patient module's negative power rail. This condition sets the LEDHI flag, which interrupts the processor. The processor then reduces the LED drive currents to avoid signal saturation.

INAMPHI — Following the INAMP programmable gain section, another comparator (U20) generates the INAMPHI interrupt. This circuit compares the signal to a 10 V reference. When the INAMP gain is set too high, the signal level exceeds 10 V, and the INAMPHI flag is set. The processor then reduces the gain of the INAMP stage to lower the signal level.

LEDLOW — If a sensor is exposed to bright light, the output of the patient module is driven negative an amount proportional to the ambient light exposure. This condition occurs because the ambient light causes an increase in the photodetector current from the sensor. The I:V converter in the patient module converts the increased current to a negative voltage.

When comparator U20 senses negative-going voltage signals more positive than its -5 V reference, it sets LEDLOW high. The processor polls the LEDLOW flag and increases drive current to the LEDs when LEDLOW is high for improved S/N ratio. This condition occurs when the patient removes the sensor from high ambient light exposure. A delay of up to 30 seconds is provided to prevent the LED current from changing in frequently changing ambient light conditions. The delay is implemented by passing the SAT signal through a fast-attack/slow-decay circuit formed by R95, R96, C74, CR8, and U27 before it reaches comparator U20. The orientation of diode CR8 causes the circuit to be sensitive only to negative-going signals.

3.4.2.5. LED Drive Circuitry

The analog switches in U19 allow the gating of separate drive voltages (VRED and VIR) for the red and IR LEDs so that the two LEDs can be run at different intensities. VRED and VIR are determined by the SAT signal level from the photodetector/patient module and set by the sample/hold subsection (SCHEMATIC PROCESSOR PCB SHEET 4, U18 and U11) on the processor board. Control signals $\overline{\text{RED}}$ and $\overline{\text{IR}}$ come from the pattern generator (SCHEMATIC PROCESSOR PCB SHEET 1, U28). Drive circuitry converts the VRED and VIR voltages to drive currents.

The voltage level at TP8 is translated to current for LED drive via a bridge driver circuit consisting of error amplifier U32 and the six signal transistors Q2 through Q7. The bridge output (J3 pins 7 and 9) goes to the back-to-back IR/red LEDs of the sensor assembly. In operation, the signals $\overline{\text{RED}}$ and $\overline{\text{IR}}$ select IR or red LED drive, determining the half of the bridge circuit that is active and forward biasing either the red or IR LED; Q3 and Q6 act as current boosters for U32, while Q2, Q4, Q5, and Q7 steer the current flow. The current through the LEDs is sensed by resistor R12 and fed back to pin 13 of error amp U32, thus maintaining a constant current proportional to voltage at TP8 and independent of the +5 V supply that powers the bridge. Maximum LED current is approximately 50 mA.

3.4.3. ECG Front End

Refer to SCHEMATIC PROCESSOR PCB SHEET 3 in the following discussion.

3.4.3.1. Active Filters

The ECG signal from the patient module is conditioned by 5 stages of active filtering. The total gain of the chain of active filters is approximately 32.

The ECG is first low-pass filtered by U12 and associated circuitry. The two filter poles are set at 40 Hz and the gain is equal to 1.

U6 is a switched-capacitor notch filter with a gain of 0.32. Capacitor switching frequency (NCLK) is derived from timer IC U34 (PROCESSOR PCB SHEET 1), and is set by the processor to remove AC power line interference. (See Section 3.4.3.4., Power Line Frequency Sensing.)

A second 2-pole, 40-Hz low-pass filter follows the notch filter. This filter removes the switching transients inherent in switched capacitor filter U6.

A high-pass filter (U12) with gain of 101 and cutoff frequency 0.5 Hz follows the second low-pass stage. Because this filter stage has a long time constant, a processor control input ($\overline{\text{ECGZERO}}$) resets the filter by discharging the filter capacitors. Reset occurs under the following conditions: if a lead comes loose from the patient (or the ECG signal is contaminated by patient muscle contractions), the ECG signal baseline can be driven into a railed condition. This occurs because of the high (approximately 1000) combined gain of the patient module and ECG front end filters. When the ECG baseline rises too much, the processor temporarily brings $\overline{\text{ECGZERO}}$ low to reset the filter.

3.4.3.2. Offset Amplifier

An offset amplifier (U12) biases the filtered ECG signal by +5 V so that the A:D converter can digitize the entire waveform (the A:D converter can only process positive analog signals). The output of the offset amplifier (ECG') is digitized by the A:D converter and provided as a data output by the powerbase.

3.4.3.3. Detached Lead Indicator

A 3-stage circuit composed of absolute-value amplifier U5, voltage comparator U4, and D-type flip-flop U3 generates the LEADOFF flag. The circuit examines the condition of the ECG signal at the input to the switched-capacitor notch filter U6, after it has undergone one stage of lowpass filtering.

A detached lead is sensed as follows: within the patient module, a biasing resistor network drives the ECG signal to one of the supply rails (±15 V) if one or both ECG signal leads becomes detached from the patient. If the signal is driven to the negative supply rail, it is converted to a positive voltage by absolute value amplifier U5. The output of this circuit is compared to a 10 V reference by comparator U4. A voltage in excess of 10 V drives the output of U4 low, setting and latching flip-flop U3 through NAND gate U10. When the flip-flop has latched, the LEADOFF logic signal is set high, notifying the processor that a lead has come loose. When the processor polls LEADOFF and discovers that it is at a logic high, it stops using the ECG R-wave as a gating mechanism and lights an LED on the instrument front panel to notify the user that the ECG signal has been lost.

The processor clears the flip-flop with $\overline{\text{CLRLO}}$ after a high LEADOFF signal has been recognized. NAND gate U10 is provided to latch the flip-flop during brief (intermittent) lead-off conditions.

3.4.3.4. Power Line Frequency Sensing

The mains power AC signal going into the power supply board is transformed to 9.2 VRMS and sensed by one-volt-crossing comparator U20. The one-volt-crossing detector produces the logic signal AC, which interrupts the processor at the frequency of the AC power line. This signal is used to set notch filter U6 to the line frequency, automatically adjusting for 60 Hz or 50 Hz power.

3.4.4. A:D/D:A Subsection

The A:D/D:A subsection is shown on SCHEMATIC PROCESSOR PCB SHEET 4.

The A:D/D:A subsection performs both analog to digital and digital to analog conversions. A unique feature of the design is the ability to subtract variable DC offsets and post-amplify signals prior to A:D conversion. This allows for accurate measurements of small modulation levels on large DC levels without slow-response AC coupling.

3.4.4.1. A:D Conversion

The sequence of a typical A:D conversion routine is as follows:

A) The 8088 processor selects an analog channel for conversion by writing to 8-to-1 analog multiplexer U24. Signals available for conversion are:

IR'	the demultiplexed and filtered IR detector channel signal
RED'	the demultiplexed and filtered RED detector channel signal
ECG'	the filtered ECG waveform
VCAL'	the filtered voltage from the calibration resistor within the sensor
VPS	the power supply voltage, used to determine whether the system is running on AC power or batteries and to check the battery voltage when the instrument is operating on battery power
ISEG	a voltage level from the display driver board, used to detect bad segments or light bars on the display during power-up test
VREF	approximately 10 V reference voltage used for board alignment
GROUND	analog ground potential used for board alignment.

B) Set programmable amplifier U30 gain by writing to latch U42.

C) Set desired analog offset value to be subtracted at U25, pin 2, by writing two bytes (low byte, high nybble) to 12-bit bus-compatible DAC U43 (12 bits, 0-10 V).

D) Now a scaled analog value is present at the output of programmable gain amplifier stage U37, pin 1, (TP3). The offset voltage has been subtracted by differential amplifier U25 and amplified by programmable amplifier U30 and U37. The total range of programmable gain is 1/8 to 16.

E) Triggering the sample and hold line (S/H) causes U36 to hold the scaled voltage for A:D conversion.

F) The 8088 processor begins executing a successive approximation routine (SAR).

G) The SAR performs a binary search sequence by setting up a voltage on the D:A converter U43 which is compared to the held signal voltage via comparator U29. The result of this comparison is polled by the processor via buffer U41.

H) The SAR continues until the least significant bit has been set. Each 12-bit conversion is accomplished in approximately 100 µs.

3.4.4.2. D:A Conversion

The analog sample/hold circuits formed by analog demultiplexer U18 and quad operational amplifier U11 are used to update and store the following four analog signals:

- VIR, which controls the IR LED brightness
- VRED, which controls the red LED brightness
- VOLUME, which controls the speaker volume.
- RWTHRESHOLD, not used.

In operation, the processor sets up an analog voltage on analog demultiplexer U18, pin 9, by writing to DAC U43. U18 is enabled through U18, pin 3, and the processor selects which output is written with address lines A0 through A2. When U18 is enabled, the voltage at U18, pin 9, is routed to one of the four outputs S1 through S4, charging storage capacitor C39, C41, C42, or C43. When U18 is disabled, the capacitor voltage is held by the very low leakage follower op amp U11 until the next update.

3.4.5. Timing and Control

Most processor timing and control flags are generated in circuits shown on SCHEMATIC PROCESSOR PCB SHEET 2 and 3. Processor timing is affected by two types of logic flags:

- Polled processor I/O signals
- Processor interrupts, which may occur asynchronously.

Many of these flags are discussed elsewhere in this section and all are summarized below.

3.4.5.1. Polled Processor Flags

Buffer U41 allows the 8088 processor to poll the following logic flags:

SWITCH indicates the state of the front panel switch (logic low indicates ON position)

LEADOFF indicates that an ECG lead has become detached, and that the ECG signal from the patient module was near saturation level as a result

LEDLOW indicates that LED drive currents should be increased to increase SAT S/N ratio

DACMP the output of voltage comparator U29, used in SAR A:D conversion

Four jumpers W2, W3, W4, W5, which are selectively installed to place the processor in various diagnostic modes.

3.4.5.2. Interrupt Processor Flags

AC interrupts the processor at the frequency of the AC power line

LEDHI instructs the processor to decrease the LED drive currents in the presence of ambient light to avoid SAT signal saturation

INAMPHI indicates that the INAMP gain is set too high. The processor then reduces the gain of the INAMP stage to lower the signal level to avoid saturation

TxRDY signals that UART U16 is ready to transmit another character

RxRDY signals that UART U16 has received a new character

INT real-time interrupt from interrupt controller U22

3.5. FRONT PANEL DISPLAY

Front panel display is accomplished by two circuit boards:

- Driver PCB, which contains drive circuitry for the display LEDs
- Display PCB, which contains the display LEDs and pushbuttons.

3.5.1. Driver PCB

The driver circuit board is shown on SCHEMATIC DRIVER PCB. Refer to this schematic in the following discussion.

During power-up, CR2, R10, and C11 provide a short-duration reset pulse to all latches on the driver board. This reset pulse clears all front-panel display elements.

Two different mechanisms are used to drive the display:

- digit and bargraph drivers
- drivers for the lightbars used with other front-panel indicators such as "PULSE SEARCH" and "AUDIO ALARM OFF."

3.5.1.1. Digit and Bargraph Drivers

A total of 8 components comprise the digit and bargraph displays (DIGIT 0 through DIGIT 5, BARGRAPH 0 and BARGRAPH 1). The drive signals for these displays are multiplexed.

Latch U12 and decoder U13 are used to select which digit or bargraph to update. Latch U10 and driver U11 determine which segments within the selected digit or bargraph are illuminated.

3.5.1.2. Lightbar Drivers

The lightbars are driven by latch circuitry and are not multiplexed. U3 and U8 drive lightbars with the following signals:

DP	lights decimal point in the 7-segment digital displays
ALMINH	lights AUDIO ALARM OFF lightbar
N/C	not connected
PLSSRCHLO	with PLSSRCHHI, lights PULSE SEARCH lightbar
PLSSRCHHI	with PLSSRCHLO, lights PULSE SEARCH lightbar
LOWSAT	lights LOW SAT lightbar.

U2 and U9 drive the remaining lightbars with the following signals:

HISAT	lights HIGH SAT lightbar
LOWRATE	lights LOW RATE lightbar
HIRATE	lights HIGH RATE lightbar
BATLO	lights LOW BATT lightbar
BATON	lights BATT IN USE lightbar
ECGLOST	lights ECG LOST lightbar
ECGON	lights ECG IN USE lightbar

Decoder U6 takes the select line from the processor ($\overline{\text{DISPLAY}}$) and the three low address lines from the processor (A0, A1, and A2) and uses them to select a latch for display updating.

3.5.1.3. Front Panel Controls

Decoder U6 also lets the processor select octal buffer U1, which reads the state of inputs BUTTON 0 through BUTTON 4 and control knob rotation information relayed through UP/DOWN (U/D) counter U5.

The control knob consists of a two channel optical chopper, with the two channels mechanically 90 degrees out of phase to each other, and a dual channel optical slot detector. Schmitt trigger inverters U4 are used to clean up the signals from the knob, one inverter per channel. Channel A provides the clocking pulse for U/D counter U5; Channel B provides the direction (U/D) signal.

The phase relationship between the two channels provides an UP or DOWN count command to the counter, depending on which way the knob is turned (clockwise rotation results in count-up commands).

To detect a change in the U/D counter, the processor reads the twos-complement value of the counter's output and adds it to its accumulated turns count. After it accumulates the counter value, the processor generates a signal into the LOAD line of U5 to clear it for the next count value.

3.5.1.4. Power-Up Display Element Test

Differential amplifier U7 senses the power return line of driver ICs U8, U9, and U11 by monitoring the voltage across resistor R9. The sensed voltage is proportional to the current flowing through the driver ICs. The voltage is amplified with a gain of 10 and is provided to the A:D converter as signal ISEG (PROCESSOR PCB SHEET 4, U24). The processor digitizes ISEG and uses it during the power-up display test to determine whether any display element has a shorted or open LED segment.

3.5.1.5. Speaker Driver Circuit

The sample/hold VOLUME signal from the processor (SCHEMATIC PROCESSOR PCB SHEET 4, U11) controls the amount of current going into the speaker's SPEAKER(+) lead. The TONE signal (SCHEMATIC PROCESSOR PCB SHEET 1, U38 and U9) switches FET Q2 to alternately connect or disconnect the SPEAKER(-) lead from ground. The frequency of the TONE signal determines the pitch of the sound produced. The harsh-sounding square wave of TONE is softened by filter capacitor C6. Diode CR1 suppresses transients from the inductive speaker load. Transistor Q1 supplies a current boost for the U7 operational amplifier.

3.5.2. Display PCB

The display circuit board is located immediately behind the front panel and contains the numeric LEDs, the LED indicator lamps, the control buttons and the control knob, as well as associated current limiting and pull-up resistors.

3.6. POWER SUPPLY PCB

The power supply circuitry is shown on the SCHEMATIC POWER SUPPLY PCB drawing.

The power supply board contains two switching power supplies in flyback converter configuration. The supplies are capable of providing 2 A at +5 V, 100 mA at +18 V, and 100 mA at -18 V.

Pulse width modulator (PWM) U2 controls the +5 V supply; PWM U4 controls the +18/-18 V supply. The PWMs sense the DC output voltages through their INV (pin 1) inputs and control the pulse width at the gates of switching FETs Q2/Q4 and Q3. Voltage regulator VR1 provides 5 V power and a 5 V reference to the two PWMs. Schmitt inverters U3 provide low impedance active current drive to the somewhat capacitive gates of the FET switching transistors, minimizing drain rise and fall times.

Also resident on the power supply board is one half (monitor side) of the powerbase-monitor optical link, formed by diode DS1 and phototransistor Q1.

3.7. BATTERY CHARGER PCB

The battery charger PCB is shown on the SCHEMATIC BATTERY CHARGER PCB drawing. The battery charger PCB contains two major circuits:

- ON/STDBY control circuitry
- Battery charger circuitry

3.7.1. ON/STDBY Control Circuit

The ON/STDBY control circuit is shown on the bottom portion of the schematic.

The ON/STDBY switch J1 is shown in the ON position. It does not switch power. Rather, it provides a logic control signal (SWITCH) that is polled by the main processor through a tri-state buffer (U41 on SCHEMATIC PROCESSOR PCB SHEET 4). When the processor senses a change in switch position from ON to STDBY through this signal, it executes a shutdown procedure. The ON mode is activated by bringing the gate of FET switch Q1 high, which provides a low impedance connection between power supply ground (labeled "P") and signal ground. STDBY mode is activated by cutting off Q1. Power supply voltage, VPS, may be either the battery voltage or the rectified and filtered AC voltage from the powerbase, depending on the mode of operation.

In the following sections, the circuit is examined as the ON/STDBY switch is moved first from ON to STDBY, and then as the instrument is returned to the ON state.

3.7.1.1. ON State

In the ON state, capacitor C2 is discharged. The combination of R5 and C2 forms a watchdog timer that ensures processor control over instrument power. If C2 is allowed to recharge, pin 8 of U1 will go low, flip-flop U2 will be cleared, the gate of Q1 will go low, and the connection between power and signal grounds will be broken.

The processor keeps C2 from recharging by placing a negative pulse on the power supply enable line (PSEN) at least once every 150 ms. The pulse is AC-coupled through capacitor C1, its rising edge producing a narrow positive-going pulse on U1, pins 1 and 2. The resulting low pulse on U1, pin 3 periodically discharges C2 through diode CR4. Capacitor C1 ensures that only active transitions on PSEN, not static highs or lows, have an affect on the watchdog timer. The N-200 is thus placed in the STDBY state if an abnormal condition "hangs" the processor.

3.7.1.2. ON to STDBY

The ON to STDBY transition can occur either by placing switch J1 in position 1 (STDBY), or in response to a decline in battery voltage below approximately 5.6 V.

Placing J1 in the STDBY position causes the voltage on the polled SWITCH signal to rise. If this occurs, or if battery voltage falls below 5.6 V, the processor blanks the front-panel displays and executes an infinite loop routine that does not involve pulsing PSEN. As a result, watchdog timer capacitor C2 is not discharged, U1, pin 9, voltage rises, U1, pin 8, voltage falls, and flip-flop U2 is cleared. The resulting logic low at U2, pin 5, shuts off FET Q1, placing the instrument in the STDBY state.

3.7.1.3. STDBY State

With the front panel switch in the STDBY state, VPS charges capacitor C5, and the SWITCH signal is maintained at logic high. SWITCH voltage is clamped to logic levels by protection zener diode CR8. Zeners CR1 and CR3 perform similar functions elsewhere in the circuit.

In STDBY, capacitor C2 is charged to 5 V through resistor R5.

3.7.1.4. STDBY to ON State

When the switch is moved to the ON position, C5 discharges through R7 and provides a momentary positive voltage pulse to Schmitt NAND gate U1, pins 4 and 5. In response, U1, pin 6, falls to logic low, discharging capacitor C2 through diode CR5, and setting D-type flip-flop U2. When the flip-flop is set, U2, pin 5, goes to logic high, placing positive voltage on the gate of FET switch Q1. Positive gate voltage on Q1 creates a low-resistance path between signal ground and power ground. As the switched voltage pulse from C5 discharges through R7, U1, pin 6, returns to a logic high, and C2 (the watchdog timer) begins recharging. The processor again begins to periodically discharge C2 to maintain the instrument in the ON state.

3.7.1.5. Voltage Regulator

Micropower voltage regulator U3 provides 5 V power to the battery charger PCB. Battery charger and ON/STDBY sensing circuitry is always on as long as the battery maintains sufficient voltage. Total current drain for the circuits on this board is approximately 40 µA.

3.7.1.6. Power-On Time Delay

A time delay provided by CR2, R6, and C3 at the gate of Q1 allows the power supplies to return to ground potential on occasions when the switch is cycled rapidly. Without this time delay, cycling the switch from ON to STDBY and back to ON might not allow the power supply voltage to fall far enough to generate a reliable power-up reset pulse to the processor (SCHEMATIC PROCESSOR PCB, SHEET 1, power-up reset circuit R1, CR1, and C19).

3.7.2. Battery Charger Circuit

Battery charger circuitry is shown in the upper part of the schematic.

AC power VCB+ and VCB- (12.5 VRMS) is taken from one of the power supply transformer secondary windings. It is rectified through diode bridge CR6 and filtered by C7 to provide a positive voltage for voltage regulator VR1. Current sensing resistor R15 provides current limiting through Q2 and Q3, cutting output voltage when current draw increases above 375 mA. Trimmer potentiometer R12 adjusts the nominal battery charging voltage to 7.1 V at TP5.

Diode CR9 prevents back-discharge through the regulating circuit when AC power is removed. With AC power disconnected, battery voltage can vary between 6.6 V and 5.6 V.

3.8. POWERBASE

The powerbase contains electronics for data communications for the N-200. It is composed of a mother PCB and three daughter PCBs.

3.8.1. Mother PCB

The mother board is shown in the SCHEMATIC MOTHER PCB POWERBASE.

The mother board provides power for the rest of the powerbase electronics. Bridge rectifier U2 charges filter capacitor C1. The AC voltage supplied at AC(±) is typically 7.5 V RMS. Voltage regulator U3 and current booster Q1 form a linear regulator that lowers the rectified AC voltage to +5 V.

Portions of the powerbase analog circuitry require ±15 V power. DC:DC converter U1 derives these voltages from the +5 V supply. U4 and U5 regulate these voltages down to ±12 V for use in the RS232 serial port.

Diode CR1 and phototransistor Q2 form one half (powerbase side) of the powerbase-monitor optical link.

3.8.2. Upper and Lower Daughter PCBs

The upper and lower daughter PCBs comprise the digital portion of the powerbase electronics.

3.8.2.1. Upper Daughter PCB

In the upper daughter PCB, 8085 processor U5 is driven by a 6.144 MHz crystal. A watchdog timer comprised of U6, C7, CR1, R5, Q1, R6, and C8 monitors the Serial Output Data (SOD) signal from U5, pin 4. If SOD does not produce a positive pulse within any 100 ms period, the watchdog timer sets the trap pin (U5, pin 6) which causes the 8085 to reset to address 0. Delay circuit CR2, R9, and C10 provides reset on power up.

Addresses presented on the multiplexed address/data bus of U5 are held by latch U2 when ALE (U5, pin 30) pulses high. 16-kbyte EPROM U4 is mapped starting at address 0, and 8-kbyte RAM U3 is mapped starting at HEX 4000. I/O for the upper daughter PCB is memory-mapped. Addresses are decoded on the lower daughter PCB.

Buffer U1 reads several digital signals:

- Four switches S1 through S4:

  —S1 and S2 (ZERO and FULL) set zero and full-scale on all analog outputs

  —S3 (TREND) initiates a TREND printout

  —S4 (EVENT) initiates an EVENT printout

- Jumpers W1 and W2, which, when installed, place the system in various diagnostic modes

- SCALE, which is the output of switch SW1 (SCHEMATIC MIDDLE DAUGHTER PCB POWERBASE), sets the SAT analog output range (0-100% or 50-100%)

- ECGTRIG, which is generated with every R-wave when an external ECG monitor is used (SCHEMATIC MIDDLE DAUGHTER PCB POWERBASE, U7, pin 7).

3.8.2.2. Lower Daughter PCB

U6 and U7 provide address decoding for all devices in the powerbase. I/O functions begin at HEX 8000.

Timer circuit U4 generates the real-time interrupt RST7.5 (U4, pin 10). U4 also produces the baud rates for UARTs U2 and U5. U5 drives the powerbase side of the monitor-powerbase optical link at 19.2 kbaud. Circuit elements associated with U5 provide signal conditioning for transmitting and receiving on the optical communication link. The link's LED and phototransistor are shown on the SCHEMATIC MOTHER PCB POWERBASE drawing.

U5, pin 23 ($\overline{RTS}$) is set low in software when the instrument is in an alarm condition, producing a logic high on U8, pin 11 (ALMOUT).

UART U2 drives the external RS232 interface and the fiber-optic output CR1. Level translator U3 performs the voltage level shift required for the TTL-RS232 interface. RxRDY (U2, pin 14) is returned to the main processor as RST5.5. Baud rates for both UARTs are derived from timer U4 (pins 13 and 17).

Buffer U1 reads 8-bit DIP switch S1, which is used to select the baud rate and data transmission format.

Connector J8 is a 9-pin miniature D type for the RS232 data link.

3.8.3. Middle Daughter PCB

The middle daughter board (shown on SCHEMATIC MIDDLE DAUGHTER PCB POWERBASE) contains all of the analog circuitry for the powerbase. For purposes of discussion, the board can be divided into two portions:

- the sample/hold circuit, with its associated DAC and analog demultiplexer
- the ECG input circuit with self-adjusting threshold. This circuit triggers processor U5 on the upper daughter board whenever an external ECG signal appears

3.8.3.1. Sample/Hold Circuit

Bus-compatible 8-bit DAC U5 is provided with a reference voltage of approximately -10 V by negative voltage regulator U6. Potentiometer R11 trims the output voltage of U1, pin 6, to +10.00 ± 0.02 V when DAC gain is set to maximum (the U1-U5 combination inverts the reference voltage). Switch SW1 selects a full scale analog output voltage of 1 V or 10 V by switching in the voltage divider formed by R2, R5, and R6.

U4 is a 1-to-8 bus-compatible analog demultiplexer. DAC output at U4, pin 9, feeds through to the selected output: U4 pin 5, 6, 7, or 8. Each output drives a separate sample/hold circuit made up of storage capacitors C4 through C7 and FET-input operational amplifiers U2 and U3. Zener diodes at the outputs of the sample/hold amplifiers protect against external short-lived transients. The 1 kohm output resistors quell oscillations which may occur when driving highly capacitive loads.

3.8.3.2. ECG Output

The ECG sample/hold channel is bidirectional. It differs from the other three channels in that the output signal is AC coupled (at a corner frequency of 0.5 Hz) to unity-gain buffer U2. Resistor R12 buffers the output of the unity-gain buffer when signals enter the ECG bidirectional port (J3). Incoming ECG signals are AC coupled through C16 and R25 to two parallel circuits:

- unity-gain buffer U3
- a peak follower circuit (composed of U2, CR9, C17, R27, and U3) with slow decay that stores the peak value of the R-wave from one peak to the next.

The peak follower circuit provides an adjustable threshold for sensing each ECG R-wave peak. Voltage comparator U7 produces a positive voltage pulse (ECGTRIG) when the ECG input signal exceeds the adjustable threshold determined by previous peak R-wave values.

SECTION 4

TROUBLESHOOTING AND ASSEMBLY GUIDE

This section first discusses some potential difficulties, their possible causes, and suggestions for resolving them that do not require disassembly of the instrument. If the difficulty persists after following these suggestions, proceed to the subsections on detailed troubleshooting and disassembly. Refer if necessary to Section 5, Testing and Calibration. If qualified service personnel are not available, contact Nellcor's Technical Service Department at 1–800–NELLCOR or 415 887-5858.

NOTE: Instrument must be operating on AC power for the powerbase to be functional.

NOTE: To reset the powerbase microprocessor, disconnect and reconnect AC power.

4.1. INITIAL TROUBLESHOOTING PROCEDURES

1. The instrument does not turn on.

   - The AC power is not connected and the battery is discharged. Connect to AC power. If the problem persists, check the AC fuse. If this does not resolve the problem, contact qualified service personnel or Nellcor's Technical Service Department.

2. The instrument operates on AC power but not on the battery.

   - The battery is discharged. Fourteen hours are required to completely recharge the battery.
   - The battery pack is defective or the battery fuse is open. Contact qualified service personnel or Nellcor's Technical Service Department.
   - The battery charger is defective. Contact qualified service personnel or Nellcor's Technical Services Department.

3. The instrument operates on AC power, but the BATT IN USE indicator is always on.

   - The powerbase is disconnected from the monitor.
   - The instrument is not receiving AC power because the power cord is defective, is not connected, or is connected to a defective AC outlet. Replace the power cord, connect to AC power, or try another AC outlet.
   - The AC fuse on the rear panel is defective. Replace the fuse (see Section 4.4.1.).

4. The instrument displays an error message.

   - "Err 1" indicates defective RAM (data memory). See Section 3.4.1.1.
   - "Err 2" indicates defective ROM (program memory). See Section 3.4.1.1.
   - "Err 3" indicates a damaged display or indicator. See Sections 4.3.4. and 3.5.1.4.

WARNING: The instrument will operate if any button is pressed while "Err 3" is showing. However, because at least one segment or indicator is missing, the display or warning indicators may be incorrect. Continue to use the instrument only in an urgent situation and only if the defective segment(s) has been identified.

- "Err 4" indicates that the N-200 lost power without going through the normal shut-down procedure. Turn the ON/STDBY switch to STDBY and back to ON.

- For software version 2.49 or higher, "Err 5" indicates jumpers W1 and W4 were not installed properly. Contact qualified service personnel or Nellcor's Technical Service Department.

  Note: The instrument will operate if any button is pressed while "Err 5" is displayed.

- "Err 6" indicates that battery-backed memory contents have been lost, and the trend and event memories were erased and reinitialized. The trend and event memories will operate normally as long as the N-200 is turned on, but when the ON/STDBY switch is set to STDBY, the trend and event memories will be erased. This message may indicate that the RAM socket assembly U15 needs to be replaced. Contact qualified service personnel or Nellcor's Technical Service Department.

  Note: This message may also appear briefly when the N-200 is first turned on after the monitor EPROM has been replaced with a different version. No action is required.

- For software version 2.5 or higher, "ALL clr" indicates that the trend and event memories were erased and reinitialized. The N-200 erases and reinitializes the memories if the data have been corrupted. The memories can also be manually cleared and reinitialized. In both cases, the "ALL clr" appears. No further action is necessary. When "ALL clr" appears because the memory data were corrupted and erased, a simultaneous 5-second alarm sounds.

  Note: If the N-200 erases the trend and event memories, a message header appears on the trend graph indicating that the oldest portion of the memory was erased.

- For software version 2.5 or higher, "Err Pb" indicates the powerbase is not communicating with the monitor. Check that the powerbase is plugged in and the monitor is correctly installed on the powerbase. If the message does not disappear, contact qualified service personnel or Nellcor's Technical Service Department.

  Note: The instrument will operate if any button is pressed while "Err Pb" is displayed.

5. Perfusion indicator is not tracking pulse (PULSE SEARCH indicator is on) and saturation and pulse rate are not displayed.

   - The sensor is improperly applied to the patient or it is not plugged in. Check and correct if necessary.

   - The patient's perfusion is too poor for the instrument to detect an acceptable pulse.

     —check the condition of the patient.

     —use *C-LOCK* ECG synchronization.

—test the instrument on yourself or another patient.

—try the nasal *OXISENSOR*™ R-15.

- The sensor is damaged. Replace with another sensor.

- The patient module is damaged. Try another patient module. If no spare patient module is available, or replacement does not resolve the problem, refer to Sections 3.3 (Patient Module), 3.4.2 (Analog Front End and LED Current Drive), and 5.4 (Processor PCB Tests).

6. Perfusion amplitude indicator tracks a pulse but there is no oxygen saturation or pulse rate display.

   - The sensor is damaged (red LED). Replace with another sensor.

   - The patient's perfusion is too low to allow the instrument to measure saturation and pulse rate (fewer than three or four bars on the perfusion display).

     —check the condition of the patient.

     —use *C-LOCK* ECG synchronization.

     —test the instrument on yourself or another patient.

     —try the nasal *OXISENSOR* R-15.

   - Excessive patient motion is making it difficult for the instrument to find the actual pulse pattern.

     —use *C-LOCK* ECG synchronization.

     —set the N-200 for Mode 3 (refer to Operator's Manual).

7. Patient module cannot be connected to the instrument.

   - Incorrect type of patient module is being used. Use a *NELLCOR* N-200-series patient module.

   - The connector pins are bent. Straighten them carefully or replace the patient module (the plug is internally sealed and should not be disassembled).

8. Saturation and/or pulse rate display are changing rapidly and pulse amplitude indicator is erratic.

   - Excessive patient motion is making it difficult for the instrument to find a pulse pattern.

     —use *C-LOCK* ECG synchronization, or

     —if possible, ask the patient to remain still, or

     —check whether the sensor is securely applied and replace it if necessary, or

     —use a type of sensor that tolerates more patient motion, or

—move the sensor to a site with less movement, or

—use Mode 3 if appropriate. (Refer to the N-200 operator's manual.)

- An electrocautery unit (ECU) is interfering with performance.

  —the ECU cable and N-200 patient module are too close to each other. Move them as far apart as possible.

  —the sensor is too close to the ground pad or electrocautery site. Move sensor to a different site if possible.

  —the ECU and N-200 are plugged into a common power source. Operate the N-200 on battery, or plug it into a different AC outlet.

  —the sensor is damp or has been reused too often. Replace it with a new sensor.

  —use an *OXISENSOR* D-25, which has added insulation against electrosurgical interference.

- Ambient light may be interfering with the sensor. Shield the sensor from bright ambient light with opaque material.

9. The ECG LOST indicator is displayed.

   - Check the condition of the patient.

   - The ECG electrode or electrode cable is loose or unplugged. Check connections.

   - If the ECG signal is supplied via the patient module, the patient module may be defective. Try another patient module. If that is not possible, see Sections 3.3., 3.4.3., and 5.4.

   - If the ECG signal is provided via the rear panel connector, the input signal from the ECG monitor may be incorrect. Use 1 V/mV ECG analog output or defib sync pulse wave.

   - AC power to the powerbase may have been interrupted (this applies only if the ECG signal is being supplied via the rear panel connector).

10. When ECG is connected, pulse rate is displayed but saturation is not.

    - The patient's perfusion may be inadequate.

      —check the condition of the patient.

      —test the instrument on yourself or another patient.

      —try the nasal *OXISENSOR* R-15.

11. The pulse rate displayed by the N-200 does not correlate with that of the ECG monitor.

    - Excessive patient motion is making it difficult for the instrument to find a pulse pattern.

      —use *C-LOCK* ECG synchronization, or

—if possible, ask the patient to remain still, or

—check whether the sensor is securely applied and replace it if necessary, or

—use a type of sensor that tolerates more patient motion, or

—move the sensor to a site with less movement, or

—use Mode 3 if appropriate (refer to the N-200 Operator's Manual).

- The patient has a pronounced dicrotic notch, which causes the pulse rate to double. Try another sensor site.
- An artifact is present on the ECG monitor. Refer to the manual for that monitor.
- An electrocautery unit is interfering (refer to item number 8).

12. Oxygen saturation measurement does not correlate with the value calculated from a blood gas determination.

    - The calculation has not been correctly adjusted for the effects of pH, temperature $PaCO_2$, 2,3-DPG, or fetal hemoglobin. In general, calculated saturation values are not reliable as correlative measurements.

      —check to see that the calculations have been corrected for relevant variables. For more information, see Section 3.1.4.

    - Accuracy can be affected by incorrect sensor application or use, significant levels of dysfunctional hemoglobins, intravascular dyes, bright light, excessive patient movement, venous pulsations, electrosurgical interference, and placement of a sensor on an extremity that has a blood pressure cuff, arterial catheter, or intravascular line. Observe all instructions, warnings, and cautions in the N-200 Operator's Manual and in the directions for sensor use.

13. The oxygen saturation measurement of the N-200 does not correlate with a value measured by a laboratory CO-Oximeter.

    - Fractional measurements have not been converted to functional measurements before the comparison was made. The *NELLCOR* N-200, like other two-wavelength oximeters, measures functional saturation. Multi-wavelength oximeters, such as the IL282 CO-Oximeter and Corning oximeters, measure fractional saturation. Fractional measurements must be converted to functional measurements for comparison. The equation used to make this conversion can be found in Section VI of the N-200 Operator's Manual.

14. The OXYGEN SATURATION display is erratic and the ECG LOST display is flashing.

    - Excessive patient motion has caused the ECG electrodes to become displaced, dislodged, or disconnected from the ECG cable.

      —check the position of the electrodes and check the connections.

- The ECG cable has come loose from the patient module connector.

  —check the connection.

- If the ECG signal is coming from a bedside ECG monitor, the ECG input cable may have become dislodged from the ECG IN/OUT connector on the rear of the N-200, or from the bedside monitor.

  —check the connection.

15. Trend and event data are not available.

    - The memory back-up battery has been discharged.
    - The trend and event memory has been erased.

16. Trend or event data cannot be printed.

    - Switch settings are incorrect.

      —check the switch settings (see N-200 Operator's Manual).

    - Cables are improperly connected.

      —check the cable connections.

17. The *NELLCOR* N-9000 recorder/interface cannot be used.

    - The switch settings are incorrect.

      —check the switch settings (see N-200 Operator's Manual).

4.2. DETAILED TROUBLESHOOTING PROCEDURES

4.2.1. Failure Modes

Instrument failures can be broadly divided into two classes.

- An outright failure of a component in one of the instrument modules will cause consistently incorrect operation or no operation at all. Use the Troubleshooting Summary below as a guide to diagnosing these failures. Subsequent sections dealing with repairs to each specific module can then be used to correct the diagnosed problem.

- The second, more difficult, problem deals with intermittent, noisy, or out-of-spec performance of the instrument. While these problems may also be related to a component failure, they can also be caused in some cases by noise in the environment (such as electrocautery or "Bovie" interference), an improperly functioning sensor or misapplication of the sensor by the user. If an instrument is suspected of having substandard performance, the procedures outlined in Section 5, Testing and Calibration, should be followed to help diagnose the problem.

WARNING: The procedures in this section require tests and adjustments made with the power applied and the cover removed. These tests should only be made by qualified service personnel and adequate precaution must be taken against electrical shock.

WARNING: Adjustment procedures described in this section could affect the measurement accuracy of the instrument. To insure continued accuracy, the procedures must be performed as described using only test equipment specified in this section.

4.2.2. Troubleshooting Summary

4.2.2.1. Monitor

Symptom	Probable Diagnosis
1. INSTRUMENT COMPLETELY INOPERATIVE (AC or battery).	A. Blown AC fuse and battery discharged. Refer to Section 4.4.1. B. Blown AC and battery fuses. Refer to Sections 4.4.1 and 4.3.5. C. Failure of the switching circuitry on the charger board. Refer to Sections 5.3.4 and 3.7. D. Power supply failure. Refer to Sections 5.3.1 and 3.6. E. Logic failure on the processor board. Refer to Sections 5.4 and 3.4.
2. INSTRUMENT INOPERATIVE ON BATTERY (functional on AC).	A. Failure of battery charger circuit on the charger board. Refer to Sections 5.3.3 and 3.7.2. B. Battery failure. Refer to Sections 5.3 and 4.3.5. C. Blown battery fuse. Refer to Section 4.3.5.
3. INSTRUMENT FUNCTIONS CORRECTLY ON BATTERY, "BATT IN USE" LIGHT STAYS ON FOR AC. **NOTE**: This symptom may turn into Symptom #1 once the battery discharges.	A. Blown AC fuse. Refer to Section 4.4.1. B. AC rectifier failure on the charger board. Refer to Sections 5.3.3 and 3.7. C. AC rectifier/filter failure on power supply. Refer to Sections 5.3.1 and 3.6. D. ±18 V power supplies out of spec. Refer to Section 5.3.1.1.
4. INSTRUMENT INOPERATIVE, RANDOM STEADY DISPLAY SEGMENTS AND/OR CONTINUOUS BEEP.	A. Failure of microprocessor logic on the processor board (including the microprocessor, ROM, RAM, and associated circuitry). Refer to Sections 5.4 and 3.4. B. +5 V power supply out of spec. Refer to Sections 5.3.1 and 3.6. C. Failure of switching circuit on charger board. Refer to Sections 5.3.4 and 3.7.

Symptom	Probable Diagnosis
5. INSTRUMENT OPERATES, DISPLAY SHOWS "Err 1."	A. Failure of RAM memory on the processor board diagnosed during power up test. Refer to Sections 5.4 and 3.4.1.
6. INSTRUMENT OPERATES, DISPLAY SHOWS "Err 2."	A. Failure of ROM memory on the processor board diagnosed during power up test. Refer to Section 5.4 and 3.4.1.
7. INSTRUMENT OPERATES, DISPLAY SHOWS "Err 3."	A. Failure of an LED segment or lamp diagnosed during power up test. Refer to Section 3.5.1.4. B. ±18 V power supplies out of spec. Refer to Sections 5.3.1 and 3.6. C. Failure of D/A conversion circuitry on the processor board. Refer to Sections 5.4.6 and 3.4.4.
8. INSTRUMENT OPERATES, DISPLAY SHOWS "Err 4."	A. Loss of power without going through normal shut-down procedure. Refer to Section 3.7.1. Turn ON/STDBY switch to STDBY and back to ON. B. ON/STDBY switch is damaged. C. Instrument is inoperative on battery. Refer to Section 5.3.
9. INSTRUMENT OPERATES, DISPLAY SHOWS "Err 5."	A. Jumpers W1 and W4 not installed properly. Note: The instrument will operate if any button is pressed while "Err 5" is displayed.
10. INSTRUMENT OPERATES, DISPLAY SHOWS "Err 6."	A. Battery-backed memory contents lost; trend and event memories erased and reinitialized. Memories will operate normally while N-200 is turned on, but when N-200 is turned to STDBY, memory contents will be erased. This error message may indicate that RAM socket assembly U15 needs to be replaced. Refer to Section 5.5.10 B. "Err 6" may also briefly appear when N-200 is first turned on after monitor EPROM has been replaced with a different version. No action required.

11. INSTRUMENT OPERATES, SHOWS "ALL clr."	A. Trend and event memories erased and reinitialized, either manually or because the data were corrupted. No further action required. (When "ALL clr" appears because the memory data were corrupted and erased, a 5-second alarm sounds simultaneously.)
12. INSTRUMENT OPERATES, SHOWS "Err Pb."	A. Monitor not correctly connected to power-base. B. LED on mother PCB defective. Refer to Section 3.8.1. C. Phototransistor on power supply PCB defective. Refer to Section 3.6. Note: The instrument will operate if any button is pressed while "Err Pb" is displayed.
13. INSTRUMENT OPERATES, NO PULSE INDICATION, PULSE RATE, OR SATURATION.	A. Sensor disconnected or inoperative. Refer to Section 3.3. B. Patient module or its cable defective. Refer to Section 3.3. C. ±18 V power supplies out of spec. Refer to Sections 5.3.1 and 3.6. D. Circuit failure of the analog signal processing circuitry on the processor board. Refer to Sections 5.4 and 3.4.2. E. A/D converter circuitry failure on the processor board. Refer to Sections 5.4.6 and 3.4.4. F. Defective LED drive or amplifier on processor board. Refer to Sections 5.4 and 3.4.2.
14. INSTRUMENT OPERATES, PULSE INDICATION, NO SATURATION OR PULSE RATE DISPLAY.	A. Defective red LED on the sensor. Refer to Section 3.3. B. Defective red LED driver circuit on processor board. Refer to Section 3.4.2.5. C. Circuit failure in the RED channel of the analog processing circuitry on the processor board. Refer to Sections 5.4.5 and 3.4.2.
15. INSTRUMENT OPERATES, PULSE WAVEFORM AND SATURATION/RATE VALUES "NOISY."	A. Defective sensor or tester. Refer to Section 3.3. B. Noisy +5 or ±18 VDC power supply. Refer to Sections 5.3.1 and 3.6. C. Partial failure of the A/D conversion circuitry on the processor board. Refer to Sections 5.4.6 and 3.4.4.
16. INSTRUMENT OPERATES, BEEPER "RASPY."	A. Noisy +5 V power supply. Refer to Sections 5.3.1.2 and 3.6.

17.	INSTRUMENT OPERATES, DOES NOT TURN OFF WITH SWITCH IN "STDBY."	A. Failure of switching circuitry in charger board. Refer to Sections 5.3.4 and 3.7.1.

4.2.2.2. Powerbase

Symptom		Probable Diagnosis
1.	NO ANALOG OR DIGITAL OUTPUTS.	A. AC power disconnected. B. Picofuse blown on mother PCB. Refer to Section 3.8.1. C. Faulty transformer. Refer to Section 3.8. D. Digital circuitry on upper or lower daughter boards. Refer to Section 3.8.2.
2.	FULL SCALE AND ZERO SWITCHES WORK, BUT NO ANALOG OUTPUTS. MONITOR INFORMATION DOES NOT APPEAR ON DIGITAL OUTPUTS.	A. Phototransistor on mother PCB defective. Refer to Section 3.8.1. B. LED on monitor power supply board defective. Refer to Section 3.6.
3.	TREND/EVENT FUNCTIONS INOPERATIVE, EXTERNAL ECG INOPERATIVE, ADULT/ NEONATE ALARM SWITCH INOPERATIVE.	A. AC power disconnected. B. LED on mother PCB defective. Refer to Section 3.8.1. C. Phototransistor on power supply PCB defective. Refer to Section 3.6.
4.	NO OR INCORRECT DIGITAL OUTPUT.	A. Baud rate mismatch between powerbase and output device. Refer to N-200 Operator's Manual.

4.3. MONITOR DISASSEMBLY AND REASSEMBLY

Unless otherwise noted, the method used for reassembly of the instrument or one of its subassemblies is the reverse of that used for disassembly.

4.3.1. Top Cover Removal

Remove AC power cord from the instrument. Disconnect the powerbase. Place the instrument top-down on a flat work surface. Remove the four Phillips-head screws from the bottom of the instrument, taking care not to lose washers. Turn the instrument over with the front panel facing you. Lift off the top cover and place it on your left as shown in Figure 4–1, leaving all internal connecting cables in place. Hold the spring-loaded latches located at the back of the monitor securely in the bottom cover while the top cover is being removed. If the latches come out, reassemble them in the bottom cover.

In its opened condition, with all cables connected, the instrument may be operated normally for calibration and troubleshooting.

Figure 4-1 shows the placement of PCBs within the top and bottom covers.

- The processor PCB is on the top cover, held with two screws. There are two washers under each screw.
- The power supply PCB is on the back edge of the instrument
- The battery charger PCB is on the left side.

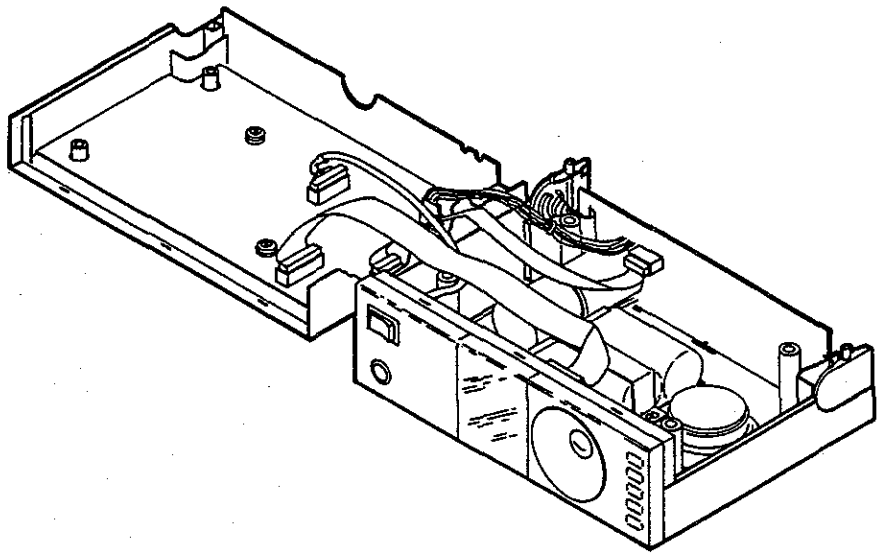


Fig. 4-1: Monitor PCB locations

4.3.2. Power Supply PCB and Battery Charger PCB Removal

The power supply PCB and battery charger PCB can be removed after the instrument top cover has been removed. Remove the two PCBs as a set by performing the following steps:

1. Disconnect all cables on the processor PCB (some connectors have retaining clips which must be removed first).
2. Cut the tie-wrap holding the large electrolytic capacitor on the power supply PCB.
3. Disconnect the 2-conductor power cable from the display driver PCB. For reassembly, verify that the red lead is on top.
4. Disconnect the battery leads and switch connector from the battery charger PCB. For reassembly, verify that the red battery lead connects to the "BATT +" terminal, the black battery lead connects to the "BATT -" terminal, and the switch connector is oriented with brown lead on top.

5. Remove the power supply PCB and battery charger PCB as one unit.

The PCBs can now be separated if necessary by disconnecting the 18-conductor flex circuit cable from the battery charger PCB.

4.3.3. Front Panel Removal

The front panel can be removed after the instrument top cover has been removed. Remove the front panel from the top cover by performing the following steps:

1. Turn the bottom cover upside-down and remove the two Phillips-head screws securing the front panel to the bottom cover.

2. Disconnect the ON/STDBY switch cable from the battery charger PCB. For reassembly, the switch connector is oriented with the brown lead on top.

3. With the bottom cover right-side up on the workbench, locate the four latches on the front panel that secure the front panel to the bottom cover.

4. Use a small blade screwdriver to disengage the front panel latches and pry them free one at a time. See Figure 4-2.

5. Pull the front panel away from the bottom cover and disconnect all cables from the driver PCB. For reassembly, verify that the 2 conductor power cable is installed with the red lead on top, the speaker cable is installed with the orange lead on top, and the ribbon cable is installed with pin 1 designators aligned.

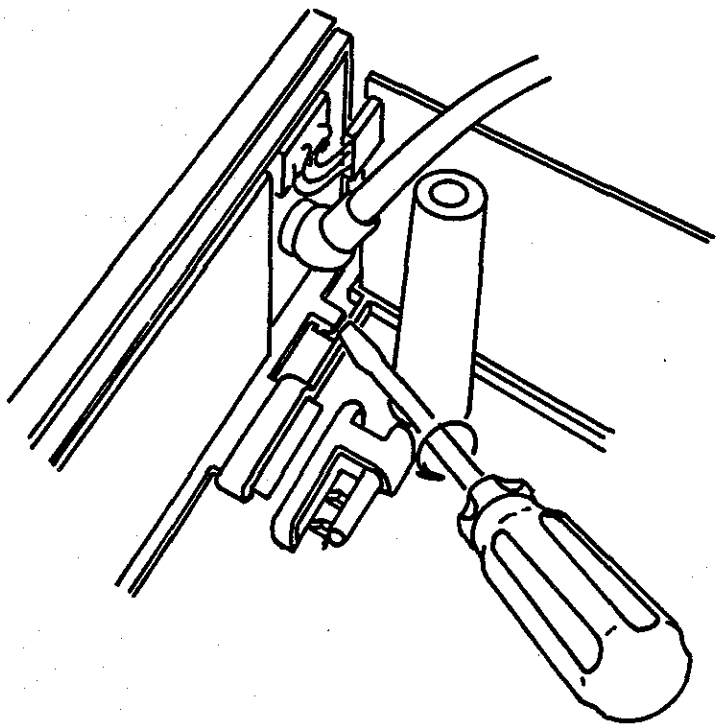


Fig. 4-2: Monitor front panel latch locations.

4.3.4. Display PCB and Driver PCB Removal

The display PCB and driver PCB are attached to the front panel; the driver PCB is nearest the instrument interior. Remove the two PCBs as a single unit by performing the following steps:

1. If not already removed, remove all connectors from the two PCBs at this time.

2. Insert a small screwdriver through the two holes above the encoder assembly and push off the encoder knob from the encoder shaft.

3. With a deep 7/16 inch hex socket, remove the encoder shaft retaining nut. Remove the encoder assembly. When replacing the encoder assembly, be sure to replace the toothed lock washer between the retaining nut and the front panel for proper knob clearance (torque on retaining nut not to exceed 15 in-lb). Verify that the encoder cable is installed with the red/white lead on top.

4. Unscrew the six Phillips-head screws securing the front panel to the display and driver PCBs. Remove the screws in two steps: first, loosen each screw part way, then go back and remove each screw completely. Note that the screws may remain in their holes, held by the plastic standoffs between the PCBs.

5. Remove the display and driver PCBs as one unit. The PCBs are assembled with component sides exposed for easy troubleshooting access. It is recommended that they not be separated unless replacement of one of the PCBs is required. If necessary, separate the two PCBs by decoupling connectors J6 and J4, then separate the PCBs by carefully prying the two snap-in standoffs apart, beginning at one end of the two-board assembly.

4.3.5. Battery Pack Removal/Fuse Replacement

The battery pack can be removed with the instrument front panel in place.

1. The in-line fuse holder and negative lead from the battery pack are secured to a clip by a tie-wrap. Cut this tie-wrap to free the battery cables. For fuse replacement, untwist halves of in-line fuse holder and replace fuse with one of same type and rating.

2. Remove the two screws from the battery retaining clip and lift out the battery pack.

4.3.6. Speaker Removal

To remove the speaker, detach the speaker connector and remove the four speaker mounting screws.

4.3.7. Top Cover Replacement

Refold the connector cables to their original contours so that the top cover fits securely without being forced. Take care that cables do not interfere with bosses or other obstructions on the cover. In particular, make sure that the shroud of processor PCB connector J4 (a five-pin header) clears the flex cable connecting the processor PCB and the battery charger PCB.

If cables have been disconnected during servicing, refer to Figure 4-1 for the order of cable replacement. Cables at the back of the unit should be connected first so that they lie below those toward the front of the unit. The order is:

1. Connect 5-conductor power cable from power supply PCB to processor PCB.

2. Connect 10-conductor ribbon cable from processor PCB to power supply PCB, noting polarity.

3. Connect patient cable from front panel LEMO connector to processor PCB, noting polarity.

4. Connect 20-conductor ribbon cable from processor PCB to driver PCB, noting polarity.

5. Replace retaining clips on all ribbon cable connectors.

NOTE: See cable interconnect diagrams, Section 9.

When refitting the top cover, note the following details:

1. Be sure that all PCBs fit properly into the alignment slots and features provided in the case. In particular, note that the power supply PCB fits into a guide on the top cover and that the charger PCB is fully seated in the slot in the bottom cover. Do not force the top cover down onto misaligned PCBs.

2. Three tabs on the top cover mate with slots on the front panel.

3. Pivot points on the side latches fit into holes in the top and bottom covers.

After the top cover has been fitted properly, turn the instrument over and replace the four screws into the bottom cover in the following manner:

1. Make sure that the washers are in place under each screw head.

2. Before tightening the screws securely, check the top cover to see that its front edge mates properly with the front panel. Press the top cover down into place if necessary.

3. When tightening the screws, be careful not to strip the threads in the plastic case by over-tightening. Recommended screw tightening torque is 16 to 18 in-lb.

4.4. POWERBASE DISASSEMBLY AND REASSEMBLY

Disconnect AC power cord before attempting disassembly. Unless otherwise noted, the method used for reassembly of the instrument or one of its subassemblies is the reverse of that used for disassembly.

4.4.1. AC Fuse Replacement

Fuses are contained inside a door above the AC power inlet on the back of the powerbase. To gain access, unplug the AC cord from the back of the powerbase and open the door by prying the top edge with a small flat-blade screwdriver.

Pull out the fuse holder on the right side to gain access to the fuse. The holder contains a 230 V, 0.5 A slo-blow fuse. Replace the fuse only with the same type and rating.

Replace the fuse holder by first making sure that the arrow on the holder points to the right, and then pressing it into place.

A removable barrel can be set to either 115 V or 230 V positions. If the barrel comes out of its holder, be sure that it is replaced so that one of the 115 V settings (United States units) is exposed to view.

Close the fuse door by exerting firm pressure against the door.

4.4.2. Powerbase Disassembly

The powerbase is disassembled by removing the four Phillips-head screws from the bottom of the unit. With the unit upright on the bench, lift off the top cover. All electronics are contained in the bottom portion of the powerbase. The solder side of the upper daughter PCB is exposed.

4.4.3. PCB Removal

The mother PCB is mounted vertically at the front of the unit. The upper, middle and lower daughter PCBs are mounted horizontally and mated to the mother PCB. The entire 4-PCB assembly can be removed as a unit by lifting the assembly out. If necessary, disconnect slip-on connectors and the 4-conductor DIN connector from mother board.

To disassemble the daughter PCBs from the mother PCB, hold the mother PCB and apply demating pressure between the bottom daughter PCB and the mother PCB. The upper and middle daughter PCBs can now be easily disconnected from the mother PCB.

4.4.4. Powerbase Reassembly

During reassembly, make sure that all pins on connector J3 on the bottom daughter PCB mate properly with the corresponding connector on the mother PCB. Also, make sure that the PCBs are seated fully in the slots and ribs provided on the backplate and on the bottom case of the powerbase.

SECTION 5

TESTING AND CALIBRATION

5.1 DESCRIPTION

This section details routine test and calibration procedures for the *NELLCOR*® N-200 pulse oximeter. Instructions for troubleshooting and repair of oximeter defects are detailed in Section 4. Refer also to Section 4 for instructions on cover removal and other access procedures. Note that certain component-level repairs require comprehensive tests of the analog section of the processor PCB to verify correct repair. If such repairs are necessary, read the appropriate parts of Section 3 that relate to the theory of operation. After the repair, verify that the circuits perform as described in Section 3, then perform the tests described in this section to verify overall instrument performance.

WARNING: The procedures in this section require tests and adjustments made with the power applied and the cover removed. These tests should only be made by qualified service personnel and adequate precautions must be taken against electrical shock.

WARNING: Adjustment procedures described in this section could affect the measurement accuracy of the instrument. To insure continued accuracy the procedures must be performed as described using only test equipment specified in this section. It is particularly important that a *NELLCOR* oximeter pocket tester be available to verify accuracy before adjustment or service is attempted. (See list of required test equipment.)

Each of the following sub-sections is designed to be used independently of the others. When any of the sub-sections is used by itself, it is required that **sub-section 5.7** be performed to assess overall system operation:

5.3 BATTERY CHARGER PCB TESTS
5.4 REGULATED POWER SUPPLY PCB TESTS
5.5 PROCESSOR PCB TESTS
5.6 POWERBASE TESTS
5.7 SYSTEM FUNCTION TESTS

WARNING: AAMI approved electrical safety testing should be performed after any repairs are completed.

The procedures assume that the N-200 Monitor and Powerbase cover have been removed and the technician has access to the inside of the instrument.

During the tests various diagnostic routines are used. The routines are invoked by accessing memory locations and inserting specified values after an enabling jumper has been installed. A memory location is selected by holding down the bottom and top front panel push buttons (AUDIO ALARM OFF and HIGH SAT) while turning the front panel selector knob until the specified memory location number appears in the OXYGEN SATURATION display. The selected location is then altered by holding in the bottom and second from the top buttons (AUDIO ALARM OFF and LOW SAT) while adjusting the selector knob until the specified number appears in the lower (PULSE RATE) display.

Example: A certain routine might be called out as (199-6). The memory location is 199 and the specified value to be entered is 6. 199 would be selected and appear in the OXYGEN SATURATION display. 6 would then be selected and appear in the PULSE RATE display.

This document is accompanied by test point maps for each circuit board to assist in locating measurement points and attachments to assist in evaluating oscilloscope traces.

5.2 REQUIRED TEST EQUIPMENT

The following test equipment is required to perform the procedures described in this section:

1. OSCILLOSCOPE, 50 mHz dual channel, 10:1 probes with 20 pf maximum input capacitance (Tektronix 465 or equivalent).

2. DIGITAL MULTIMETER (DMM), 4 1/2 digits, 0.1 % accuracy, DC volts, AC volts and ohmeter functions.

3. FUNCTION GENERATOR, 1 Hz to 1 kHz with DC level offset adjustment.

4. DC POWER SUPPLY, variable voltage 0 - 10 volts, 0 - 2 amps.

5. TEST RESISTOR, 10 ohms 10 %, 2 Watts.

6. TEST RESISTOR, 6,040 ohms 1 %.

7. TEST RESISTOR, 9,760 ohms 1 %.

8. *NELLCOR* D-25 sensor, or any *NELLCOR* flexible sensor.

9. *NELLCOR* pocket tester, model PT 2500.

10. TIMER, 0 - 60 seconds.

5.3 BATTERY CHARGER PCB TESTS

These steps verify correct operation of the battery charging circuitry, the low battery/power ON-OFF control circuit and parts of the Power Supply PCB that must be functional to conduct these tests. The tests listed below will be performed and adjustment details, if any, explained:

1. **Raw DC Voltage (both AC and battery operation)**

2. **Battery charging Voltage**

3. **Low Battery/Instrument Shutoff Voltages**

4. **ON/STDBY Switch Test**

5. **Battery Operation**

5.3.1 Raw DC Voltage

These steps test the power transformer, capacitor C2, rectifier U1 on the Power Supply PCB and the battery. If any of these components are defective the Battery Charger PCB will not function properly.

1. Verify that the power cord is disconnected from the N-200.

2. Set the ON/STDBY switch to STDBY.

3. Set the OSCILLOSCOPE as follows:

   Channel 1 : 2 V/div DC coupled.
   Sweep Rate : 10 ms/div.
   Trigger : Channel 1

4. Connect the OSCILLOSCOPE ground to the (AGND) test point on the Processor PCB.

5. Connect OSCILLOSCOPE, channel 1, input to the cathode (bar) end of CR2 on the Power Supply PCB.

6. The OSCILLOSCOPE must read "0" volts.

7. Place the ON/STDBY switch in the ON position.

8. The OSCILLOSCOPE must read between 5.2 and 6.4 volts DC with ripple and noise less than 1.50 volts p-p. NOTE: The actual DC voltage will depend on the battery voltage.

9. Connect the power cord to the N-200 and plug it into an AC outlet.

10. The OSCILLOSCOPE must read between 10 and 15 volts DC with ripple and noise less than 1.50 volts p-p. NOTE: The actual DC voltage will depend on the AC line value.

11. Disconnect the OSCILLOSCOPE from the N-200.

5.3.2 Battery Charging Voltage

Note: There are two versions of this assembly: 2270 and 6240. The test results are given for the 6240 and, if differences exist, in parenthesis ( ) for the 2270.

These steps will test the battery charging circuit consisting of CR6, VR1, Q2, Q3, and CR9. Additionally, proper adjustment of the battery charging voltage will be discussed.

1. Disconnect the AC power cord from the N-200.

2. Disconnect the RED and BLACK battery leads from the Battery Charger PCB.

   CAUTION: There is approximately 6 VDC on these connectors.

3. Connect a 1,000 ohm resistor across the DMM leads to improve measurement stability.

4. Connect the + DMM lead to the BATT + terminal on the Battery Charger PCB.

5. Connect the - DMM lead to R4 (end pointing toward the rear of the N-200 on the Battery Charger PCB). This is a convenient location for the BATT - terminal connection.

6. Connect the AC power cord to the N-200.

7. The DMM must indicate an open circuit voltage of 7.1 ± 0.02 (7.2 ± 0.002). If the voltage is out of tolerance adjust R12. R12 is located in approximately the center of the Battery Charger PCB.

8. Connect the 10 ohm 2 watt load resistor across the DMM measurement points. The DMM indication must drop to 3.75 ± 0.50 (2.50 ± 0.50) volts. If the voltage drop is not observed the current limit circuit is defective.

9. Place the ON/STDBY switch in the STDBY position.

5.3.3 Low Battery/Instrument Shut-off Voltages

These tests will verify the operation of FET Q1, associated components and microprocessor operation with regard to power control.

1. Disconnect the N-200 AC power cord.

2. Adjust the DC POWER SUPPLY to 0 VDC.

3. Connect the + DC POWER SUPPLY lead to the BATT + terminal on the Battery Charger PCB.

4. Connect the - DC POWER SUPPLY lead to R4 (end pointing toward the rear of the N-200 on the Battery Charger PCB). This is a convenient location for the BATT - terminal.

5. Connect the - DMM lead to (AGND) on the Processor PCB.

6. Connect the + DMM lead to the cathode (bar) end of CR2 on the Power Supply PCB.

7. Raise the DC POWER SUPPLY voltage 6 volts. Note: If you are using the DMM to monitor the DC POWER SUPPLY make sure to reconnect it to CR2.

8. Place the ON/STDBY switch in the ON position. Note that the N-200 powers up in a normal fashion and the BATT IN USE light is on. NOTE: The DMM will now be indicating around 5.4 volts.

9. Very slowly decrease the DC POWER SUPPLY voltage until the N-200 LOW BATT indicator light just comes on. Examine the DMM for an indication of 5.2 ± 0.05 volts. Note: If the DMM indication is low you probably decreased the DC POWER SUPPLY too fast. To repeat the test, increase the DC POWER SUPPLY back to 6 volts and then cycle the N-200 OFF and ON to reset the LOW BATT indicator.

10. Watch the DMM as you again slowly decrease the DC POWER SUPPLY voltage until the N-200 just shuts off. The DMM must indicate 5.0 ± 0.05 volts just as the N-200 shuts off. NOTE: The DMM reading will drop to approximately zero at shutoff because the power and system grounds are separated.

11. Set the ON/STDBY switch to STDBY.

12. Remove all test equipment and reconnect the battery cables to the Battery Charger PCB.

5.3.4 ON/STDBY Switch Test

These tests verify the operation of the ON/STDBY switch and the watchdog timer circuit.

1. Disconnect connector J2 from the Processor PCB (10 conductor cable).

2. Set the OSCILLOSCOPE as follows:

   Channel 1 : 5 V/div, DC Coupling
   Sweep Rate : 100 ms/div
   Trigger : Channel 1

3. Connect the OSCILLOSCOPE, ground lead, to R4 on the Battery Charger PCB (end pointing toward the rear of the N-200).

4. Connect the OSCILLOSCOPE, Channel 1, to R6 on the Battery Charger PCB (end pointing the rear of the N-200).

5. The OSCILLOSCOPE must indicate a logic low or approximately 0 volts.

6. Place the ON/STDBY switch in the ON position. The OSCILLOSCOPE trace must show a momentary logic high (approximately 5 volts) for 200 ± 50.0 ms and then return to a logic low.

7. Place the ON/STDBY switch in the STDBY position.

8. Remove all test equipment and reconnect connector J2 to the Processor PCB.

5.3.5 Battery Operation

Further verify proper battery operation by charging the batteries for 14 hours and operating the N-200 on battery power with a pocket tester attached and the alarms disabled. The N-200 must operate for a minimum of 2.0 hours.

Failure of any of the above tests indicates a malfunction and the instrument is subject to repair.

5.4 REGULATED POWER SUPPLY PCB TESTS

The following tests verify correct operation of the following components:

1. **The + 5.00 Power Supply**

2. **The ± 18.00 Volt Power Supply**

These voltages are generated by two independent power supply sections on the PCB, both consisting of pulse width modulation control chips and associated circuitry. All three outputs should be carefully checked for voltage and noise. Since the power supply is a switching type DC to DC converter it is quite possible that a component failure may not cause supply failure, but may introduce unacceptable noise levels on the output.

This procedure requires that noise measurements be made. Noise measurements may include a fine "grass" at the power supply switching frequency of 45 kHz. The "grass" component is somewhat dependent on measurement technique and the oscilloscope probe being used. The 45 kHz "grass" is not part of these noise measurements. The noise of concern in these measurements is between 100 and 1000 Hz. Some display LED load-switching variations may also be observed. This component is acceptable if it is within the 100 mV p-p limits. If a noise problem is suspected and not identified in the following tests, repeat the noise tests at an elevated temperature of 40 deg. C with the cover in place or 50° C without the cover.

1. Connect the N-200 to an AC power source and set the ON/STDBY switch to ON.

2. Connect the - DMM lead to (AGND) on the Processor PCB.

3. Connect the + DMM lead to the cathode (bar) of CR1 on the Power Supply PCB. The DMM must indicate 5.00 ± 0.15 volts DC.

4. Place the + DMM lead to FB2 on the Power Supply PCB. The DMM must indicate 18.00 (+1.8/ - 0.5 or 17.50 to 19.80 volts).

5. Place the DMM + lead to pin E5 on the Power Supply PCB. The DMM must read -18.00 (+ 0.50/- 1.80 or -17.50 to -19.80 volts).

6. Remove the DMM from the circuit.

7. Set the OSCILLOSCOPE as follows:

   Channel 1 : 100 mV/div, AC Coupling
   Sweep Rate : 50 ms/div
   Trigger : Channel 1

8. Connect the OSCILLOSCOPE ground to (AGND) on the Processor PCB.

9. Connect the OSCILLOSCOPE, Channel 1, lead to CR1 cathode (bar) on the Power Supply PCB. The lower frequency noise must not exceed 100 mV p-p.

10. Connect the OSCILLOSCOPE, Channel 1, lead to FB2 on the Power Supply PCB. The lower frequency noise must not exceed 100 mV p-p.

11. Connect the OSCILLOSCOPE, Channel 1, lead to pin E5 on the Power Supply PCB. The lower frequency noise must not exceed 100 mV p-p.

12. Remove the all test equipment from the N-200 and place the ON/STDBY switch in the STDBY position.

5.5 PROCESSOR PCB TESTS

The following tests are designed to test processor PCB operation. The following circuits will be tested in this section and adjustment details explained, as necessary:

1. **Processor PCB Voltage Regulation.**
2. **Calibration Resistor Determination**
3. **LED Intensity Control**
4. **Input Amplifier (INAMP) automatic gain.**
5. **Sync Detector Alignment.**
6. **IR Channel Gain.**
7. **RED Channel Gain.**
8. **ECG Processor**
9. **A:D/D:A Alignment.**
10. **Clock/Calendar Lithium Battery**

Prepare the N-200 for testing by performing the following procedures:

1. Place the ON/STDBY switch to the STDBY position.

2. Place a jumper wire in location W3 on the Processor PCB.

   WARNING: the jumper must be removed at the end of the Processor PCB tests. Failure to remove the jumper could allow the operator to accidentally interrupt normal software operation while the instrument is in use.

5.5.1 Processor PCB Voltage Regulation

This test verifies voltage regulation of the Processor PCB "on-board" regulators VR1 (+15), VR2 (-15), VR3 (+5), and VR4 (-5).

1. Place the ON/STDBY switch in the ON position.

2. Connect the - DMM lead to (AGND) on the Processor PCB.

3. Connect the + DMM lead to the VR1 output lead. The DMM must read 15.00 ± 0.750 volts (14.250 to 15.750).

4. Connect the + DMM lead to the VR2 output lead. The DMM must read -15.00 ± 0.750 volts (-14.250 to -15.750).

5. Connect the + DMM lead to the VR3 output lead. The DMM must read 5.00 ± 0.250 volts (4.750 to 5.250).

6. Connect the + DMM lead to the VR4 output lead. The DMM must read -5.00 ± 0.250 volts (-4.750 to -5.250).

7. Disconnect all test equipment except the jumper on W3.

5.5.2 Calibration Resistor Determination

The following test will verify the operation of the Sensor Calibration Resistor determination circuit and required microprocessor involvement. Known values of resistance are placed across the circuit input and the resulting "index" voltages are measured.

1. Connect the 6040 OHM 1.0% TEST RESISTOR from U27 pin 10 on the Processor PCB to (AGND). Alternate method is to place the resistor across pins 1 and 6 of the patient module if it is plugged in to the N-200.

2. Using the N-200 Control Knob select memory location 9 in the OXYGEN SATURATION display (see the first page of this section for details). Examine the location, in the PULSE RATE display, for a value of 64.

3. Replace the 6040 OHM 1.0% TEST RESISTOR with the 9760 OHM 1.0% TEST RESISTOR.

4. Examine location 9 again for a value of 84. These two numbers verify the range limits of the circuit which generates voltage VCAL.

5. Remove all test equipment except the W3 jumper.

5.5.3 LED Intensity Control

This procedure uses normal system components to test circuit operation. A D-25 Sensor (or equivalent disposable or flexible sensor) is used to examine LED intensities. The red LED is used to verify intensity modulation caused by the LED Intensity Control Circuit. This test also verifies operation of the LEDLOW flag (output at U20 pin 14), and the LEDHI interrupt (output at U20 pin 3).

1. Connect a patient module to the N-200.

2. Connect the Sensor to the patient module and notice that the Red LED is visible.

3. Slowly move the LED in proximity to the optical sensing element of the sensor. Notice, as the LED approaches the optical sensor, LED intensity will decrease.

4. Open the sensor and notice that the LED intensity will increase after a few moments.

5. Repeat step 3 and the intensity will again decrease. This "hunting" is an indication that the microprocessor is in proper control of LED intensity.

5.5.4 Input Amplifier (INAMP) Automatic Gain

1. Disconnect the Patient Cable connector J3, from the Processor PCB.

2. Invoke the diagnostic loop (190-1). (See page 1 of this section for details).

3. Set the FUNCTION GENERATOR as follows:

   Waveform : Sine
   Frequency : 10.0 Hz
   Amplitude : 2 V p-p

4. Connect the FUNCTION GENERATOR ground to (AGND) on the Processor PCB.

5. Connect the FUNCTION GENERATOR output to TP-6 on the Processor PCB.

6. Set the OSCILLOSCOPE as follows:

   Channel 1 : 5 V/div DC Coupled.
   Channel 2 : 2 V/div DC Coupled.
   Sweep Rate : 10 msec/div.
   Trigger : Channel 1, auto

7. Connect the OSCILLOSCOPE ground to (AGND) on the Processor PCB.

8. Connect the OSCILLOSCOPE, Channel 1, to TP-7 on the Processor PCB.

9. Select memory location 193. Depress AUDIO ALARM and LOW SAT buttons and set the value of location 193 to "0." The displayed sine wave will be <1 volt p-p. Slowly increase the value of location 193 and notice that the amplitude of the sine wave will increase. When the value of location 193 reaches approximately 150, the displayed sine wave amplitude will saturate at approximately 30 volts p-p (this represents the ± 15 volt opamp rails).

10. Adjust location 193 value to 0.

11. Connect the OSCILLOSCOPE, Channel 2, input to U20 pin 2. Note that Channel 2 displays a TTL level of approximately 0 volts.

12. Slowly increase the value of 193 until the Channel 1 waveform reaches approximately 20 volts p-p. Continue to increase the value and notice that there will be a positive pulse appear on Channel 2 which corresponds to the the area of the positive sine wave cycle which exceeds an approximately +10 V peak, i.e.; 20 V p-p. This positive pulse is the microprocessor flag INAMPHI which initiates INAMP gain reduction.

5.5.5 Sync Detector Alignment

1. Prior to performing this test make sure the N-200 has been operating more than 5 minutes.

2. Select memory location 193 and adjust its value until OSCILLOSCOPE Channel 1 is 10 volts p-p.

3. Connect Channel 2 to TP-10 and increase Channel 2 gain to 20 mV/div (or higher resolution if available), AC Coupled. The signal will be "fuzzy" but the 10 Hz component will be evident. NOTE: A Low Pass Filter can be used to remove the 50 kHz noise as long as the pass band includes up to 15 kHz.

4. Adjust R123 to null the 10 Hz component of the signal viewed on Channel 2. The final null must be less than 10 mV p-p.

5. Connect the OSCILLOSCOPE Channel 2 to TP-9 and verify that TP-9 signal is also less than 10 mV p-p.

5.5.6 IR Channel Gain

1. Set the FUNCTION GENERATOR as follows:

   Function : Sinewave
   Frequency : 10 Hz
   Output : 0.5 V, zero offset

2. Connect the FUNCTION GENERATOR ground to (AGND).

3. Connect the FUNCTION GENERATOR output to U7 pin 12 (IR Channel input).

4. Set the OSCILLOSCOPE as follows:

   Channel 1 : 2 V/div, DC Coupled
   Sweep Rate : 200 ms/div
   Trigger : Channel 1, auto

5. Connect the OSCILLOSCOPE, Channel 1, to TP-9 (IR Channel output) on the Processor PCB. Verify the signal level measures 5 to 7 volts p-p.

5.5.7 RED Channel Gain

1. Connect the FUNCTION GENERATOR output to U13 pin 12 (RED Channel input).

2. Connect the OSCILLOSCOPE, Channel 1, to TP-10 (RED Channel output) on the Processor PCB. Verify the signal level measures 10 to 14 volts p-p.

3. Remove all test equipment except the W3 jumper.

5.5.8 ECG Processor

The following tests verify the correct operation of the components of the ECG signal conditioning circuits. The patient module must be disconnected for these steps.

1. Set the FUNCTION GENERATOR as follows:

   Function : Sine Wave
   Frequency : 10 Hz
   Output : Minimum

2. Connect the FUNCTION GENERATOR ground to (AGND).

3. Connect the FUNCTION GENERATOR output to the top of R65.

4. Set the OSCILLOSCOPE as follows:

   Channel 1 : 0.5 V/div, DC Coupled
   Channel 2 : 5 V/div, DC Coupled
   Sweep Rate : as necessary
   Trigger : as necessary

5. Connect the OSCILLOSCOPE, Channel 1, to the top of R65 to monitor the FUNCTION GENERATOR output.

6. Connect the OSCILLOSCOPE, Channel 2, to TP-11 (ECG Channel output) on the Processor PCB.

7. Adjust the FUNCTION GENERATOR for an output of 16.0 ± 1 volts p-p as seen on the OSCILLOSCOPE, Channel 2.

8. Examine the OSCILLOSCOPE, Channel 1, and note the amplitude.

9. Adjust the FUNCTION GENERATOR to the following frequencies. Verify the amplitude of the OSCILLOSCOPE, Channel 1, does not vary from that noted in step 8 and Channel 2 conforms to the listed values which represent the ECG processing circuit bandpass limits.

Frequencies in Hertz	**Channel 2 limits in volts p-p**
0.5	11 ± 3
10.0	16 ± 1
40.0	11 ± 3
50.0	7 ± 3

10. Slowly adjust the FUNCTION GENERATOR from 50 to 70 Hz and notice that the OSCILLOSCOPE, Channel 2 indicates the action of the 60 Hz Notch Filter by a complete amplitude reduction or a null at 60 Hz.

11. The final (positive offset) stage of the ECG Channel can be qualified by adjusting the FUNCTION GENERATOR to 10 Hz and noting that the majority of the signal on the OSCILLOSCOPE, Channel 2, is above zero (about 80%).

12. Disconnect all test equipment except the W3 jumper.

13. To test the detached lead detector circuit, set the DC POWER SUPPLY to 15 volts.

14. Connect the + DC POWER SUPPLY lead to (AGND).

15. Connect the -DMM lead to (AGND).

16. Remove instrument from diagnostic loop by setting (190-0).

17. Connect the + DMM lead to U3 pin 9 the LEADOFF flag generator. The DMM must read approximately zero volts. If the DMM indicates around 5 volts, barring circuit malfunction, it probably means that the Detached Lead Detector Circuit has been triggered by some extraneous influence. This condition can be remedied by momentarily grounding R65.

18. Touch the - DC POWER SUPPLY lead to the top of R65 for a moment and verify the DMM now indicates approximately 5 volts. This verifies that the Detached Lead Detector Circuit is functioning.

19. To test the line frequency sampling circuit, set the OSCILLOSCOPE as follows:

    Channel 1 : 2 V/div, DC Coupled
    Sweep Rate : 5.0 ms/div
    Trigger : Line, auto

20. Connect the OSCILLOSCOPE ground to (AGND).

21. Connect the OSCILLOSCOPE, Channel 1, to U20 pin 15 and verify that the indicated square wave, syncs with the 60 Hz line, has a period of 16 ms and an amplitude of about 4 volts p-p. This verifies the operation of the line frequency sampling circuit.

22. Disconnect all test equipment except the W3 jumper.

5.5.9 A:D/D:A Alignment

These tests verify the correct operation of the multiplexer, automatic offset control, and digitizing circuitry.

1. Set up the following memory locations as specified:

    190-1
    195-7
    196-8
    197-0
    198-0

2. Connect the -DMM lead (of a 4 1/2 digit DMM) to (AGND) on the Processor PCB.

3. Connect the +DMM lead to TP-2 on the Processor PCB.

4. Adjust R117 on the Processor PCB for a reading of 0.0000 on the DMM.

5. Connect the +DMM lead to TP-3 on the Processor PCB.

6. Read and record any offset voltage, and its polarity, at TP-3 on the Processor PCB

7. Connect the +DMM lead to TP-1 on the Processor PCB.

8. Set memory location 195-6. Note that the DMM now indicates around 10 volts. Record the exact voltage.

9. Algebraically add the voltages recorded at TP-1 (step 8) and TP-3 (step 6).

   Example 1:
   a. TP-3 voltage in step 6 = -0.017 volts
   b. TP-1 voltage in step 8 = 9.997 volts
   c. The algebraic sum will be 9.997 - 0.017 or 9.980

   Example 2:
   a. TP-3 voltage in step 6 = +0.017 volts
   b. TP-1 voltage in step 8 = 9.997 volts
   c. The algebraic sum will be 9.997 + 0.017 or 10.014

10. Connect the +DMM lead to TP-3 on the Processor PCB.

11. Adjust R116 to read the value calculated in step 9.

12. Connect the +DMM lead to TP-5 on the Processor PCB.

13. Set the following memory locations as specified.

    197-255
    198-15

14. Adjust R130 to read 9.997 to 9.998 volts DC.

15. GLPT all trimpots to prevent vibrational shifts.

16. REMOVE JUMPER W3.

    WARNING: Leaving JUMPER W3 in the circuit could affect normal instrument operation.

17. Remove all test equipment and place the ON/STDBY switch in the STDBY position.

18. Reconnect the connector to J3 on the Processor PCB.

5.5.10 Clock/Calendar Lithium Battery Test

The clock/calendar assembly U15 includes a lithium-powered clock chip mounted in the center of the special socket under the RAM chip. Battery failure will cause a momentary "Err 6" display upon instrument power-up and loss of trend data. The combination of these two events is not exclusive to lithium battery failure but suggests this may be a possibility. The following steps describe testing this battery.

1. Place the ON/STDBY switch to STDBY to prevent the power supply from masking the lithium voltage value.

2. Connect the – DMM lead to U15 pin 14 (– lithium battery voltage).

3. Connect the + DMM lead to U15 pin 28 (+ lithium battery voltage).

4. The DMM must indicate between 2.0 and 3.6 volts. Nominal voltage will be 2.8. Note: if pins 14 and 28 are accidently shorted during this procedure, a temporary "Err 6" will result on the first power-up after the test.

Note: When the clock/calendar assembly (containing the lithium battery) is replaced, a momentary "Err 6" message will occur the first time the monitor is subsequently powered-up.

5.6 POWERBASE ALIGNMENT

The following tests detail the methods to calibrate the zero and span for the analog outputs.

1. Connect the AC power cord.

   WARNING: ELECTRICAL SHOCK HAZARD. When the powerbase cover is removed, AC power voltages are exposed. Do not place fingers or metal tools in contact with AC power sources.

2. Place the ON/STDBY switch in the ON position.

3. Connect the DMM to the SAT output jack (J5 on the Middle Daughter PCB schematic) rear of the N-200. The jack is a 3/32" phone plug signal to tip and ground to ring.

4. Set the SaO_2% (#1) dipswitch on the rear of the N-200 to the 0-100 position.

5. Set the VOLT (#2) dipswitch on the rear of the N-200 to the 0-1 position.

6. Press the ZERO button on the rear of the N-200. Examine the DMM for a 0.00 ± 0.01 volts indication. If necessary adjust R3 on the Middle Daughter PCB. (This adjustment is accessible through the hole marked "0V" in the Upper Daughter PCB.)

7. Press the FULL button on the rear of the N-200. Examine the DMM for a 1.00 ± 0.01 volts indication. If necessary adjust R2 on the Middle Daughter PCB. (This adjustment is accessible through the hole marked "1V" on the Upper Daughter PCB.)

8. Set the VOLT (#2) dipswitch on the rear of the N-200 to the 0-10 position.

9. Press the FULL button on the rear of the N-200. Examine the DMM for a 10.00 ± 0.01 volts indication. If necessary adjust R11 on the Middle Daughter PCB. (This adjustment is accessible through the hole marked "10V" on the Upper Daughter PCB.)

10. Remove all test equipment and place the ON/STDBY switch in the STDBY position.

5.7 SYSTEM FUNCTION TEST

The following tests allow for further circuit verification including using signals from the pocket tester:

1. **AC Operation**
2. **Battery Operation**
3. **Adult/Neonatal Alarm Limits**
4. **Pocket Tester Operation**
5. **Alarm Limits Adjustment**
6. **Temporary Alarm Silence**
7. **Disabling the Audible Alarm**
8. **Powerbase-to-Monitor Communication**
9. **Monitor-to-Powerbase Communication**
10. **Middle Daughter PCB Verification**

5.7.1 AC Operation:

1. Connect a patient module to the N-200.

2. Place the ON/STDBY switch in the ON position and verify that the N-200 operates normally:

   a. The N-200 emits a "beep."

   b. All displays light momentarily.

   c. All displays flash in a "rolling" fashion.

   d. The N-200 goes into PULSE SEARCH mode.

5.7.2 Battery Operation:

1. Disconnect the AC power cord from the N-200 and note that the BATT IN USE indicator illuminates.

2. Reconnect the AC power cord and verify that the BATT IN USE indicator extinguishes.

5.7.3 Adult/Neonatal Alarm Limits:

1. Locate the series of eight DIP switches on the back panel of the N-200. Make sure that DIP switch #1 is in the up position (adult limits).

2. Push and hold the HI SAT button. Verify that the OXYGEN SATURATION display shows an alarm limit of "100."

3. Push and hold the HI RATE button. Verify that the PULSE RATE display shows an alarm limit of 140.

4. Use a slender, nonmetallic object to move the DIP switch #1 to the down position (neonatal limits).

5. Push and hold the HI SAT button. Verify that the OXYGEN SATURATION display shows an alarm limit of 95.

6. Push and hold the HI RATE button. Verify that the PULSE RATE display shows an alarm limit of 200.

7. Return DIP switch #1 to the up position (adult limits) and place the ON/STDBY switch in the STDBY position.

5.7.4 Pocket Tester Operation

1. Connect the *NELLCOR* PT-2500 pocket tester to the patient module.

2. Place the ON/STDBY switch in the ON position. Notice that after about 10 seconds delay the N-200 will begin to follow the artificial pulse and saturation values and start giving a proper SaO_2% and Pulse Rate as per the pocket tester label.

3. Verify that the LOW SAT and LOW RATE alarms are active as follows: the OXYGEN SATURATION and PULSE RATE displays and the indicators next to the LOW SAT and LOW RATE buttons are flashing, and the audio alarm is sounding. NOTE: The alarms may be temporarily silenced while making these tests by depressing the AUDIO ALARM OFF button.

4. Set the OSCILLOSCOPE as follows:

   Channel 1 : 0.200 V/div, AC coupling
   Sweep Rate : 0.100 ms/div
   Trigger : Channel 1, auto

5. Connect the OSCILLOSCOPE ground to (AGND) on the Processor PCB.

6. Connect the OSCILLOSCOPE, channel 1, to TP-6 on the Processor PCB.

7. Examine the OSCILLOSCOPE trace to verify that the signal complies with that shown in Attachment 1 Waveform "A." The signal is essentially centered around zero volts and has a period of 333 ± 10 microseconds, and represents typical "on-off" sequences of one of the sensor LEDs. The pulse amplitude not including transient spikes must be 260 ± 100 millivolts.

8. Set the OSCILLOSCOPE as follows:

   Channel 1 : 2 V/div, DC coupling
   Channel 2 : 2 V/div, DC coupling
   Sweep Rate : 200 ms/div
   Trigger : Channel 1, auto

9. Connect the OSCILLOSCOPE, channel 1, to TP-9 on the Processor PCB.

10. Connect the OSCILLOSCOPE, channel 2, to TP-10 on the Processor PCB.

11. Examine the OSCILLOSCOPE traces to verify that the signals comply with those shown on Attachment 1 Waveform B. The DC offset for the channel 1 signal can be between 4 and 5 volts. The DC offset for the channel 2 signal can be between approximately 8 and 10 volts. The signal amplitude may vary from 100 to 200 millivolts p-p but the important point is that Channel 1 (TP-9 IR) is 1/2 the amplitude of Channel 2 (TP-10 RED).

12. Simultaneously, press the HI SAT and the AUDIO ALARM OFF buttons. While holding the buttons in, adjust the front panel control knob until the OXYGEN SATURATION display reads memory location 24. Examine the PULSE RATE display and verify that it reads between 32 and 44. This reading is the Input Amplifier gain setting.

13. If the N-200 meets all of the above tests disconnect the test equipment (not the patient module and pocket tester) and continue with the following steps. If the preceding steps are not met, the instrument is not functioning properly and must be repaired.

5.7.5 Adjusting Alarm Limits:

1. Record the number displayed in the OXYGEN SATURATION window. Press and hold the LOW SAT button and slowly turn the control knob counter-clockwise. Verify that the LOW SAT indicator goes out when the OXYGEN SATURATION display reaches the number noted in the beginning of this step.

   Continue turning the control knob until the value in the OXYGEN SATURATION window is 75 or less.

2. Record the number displayed in the PULSE RATE window. Press and hold the LOW RATE button and slowly turn the control knob counter-clockwise. Verify that the LOW RATE indicator goes out when the PULSE RATE display reaches the number noted in the beginning of this step.

Continue turning the control knob until the value in the PULSE RATE window is 40 or less.

3. Press and hold the HI SAT button and turn the control knob counter-clockwise. Verify that when the value in the OXYGEN SATURATION display goes below the number recorded in step 1, the HI SAT indicator begins flashing and the audio alarm sounds.

   Still holding the HI SAT button, turn the control knob clockwise until the alarms stop.

4. Press and hold the HI RATE button and turn the control counter-clockwise. Verify that when the value in the PULSE RATE display goes below the number recorded in step 2, the HI RATE indicator begins flashing and the audio alarm sounds.

5. Place the ON/STDBY switch in the STDBY position.

5.7.6 Temporary Alarm Silence:

1. Place the ON/STDBY switch to ON. Notice that after a few seconds delay the N-200 will begin to follow the artificial pulse and saturation values and start giving a proper SaO_2% and Pulse Rate as per the pocket tester label.

2. Verify that the LOW SAT and LOW RATE alarms are active as follows: the OXYGEN SATURATION and PULSE RATE displays and the indicators next to the LOW SAT and LOW RATE buttons are flashing, and the audio alarm is sounding.

3. Press the AUDIO ALARM OFF button.

4. Verify that the red AUDIO ALARM OFF indicator and the audio alarm go off for 60 ± 2.0 seconds.

5.7.7 Disabling the Audible Alarm:

1. Hold the AUDIO ALARM OFF button down and turn the control knob clockwise until "OFF" appears in the OXYGEN SATURATION display.

2. Verify that the AUDIO ALARM OFF indicator begins to flash, the LOW SAT and LOW RATE indicators remain flashing, and the audio alarm is silent.

3. Reactivate the audio alarm by pressing the AUDIO ALARM OFF button again. Verify that the AUDIO ALARM OFF indicator goes out and the alarm starts sounding.

4. Place ON/STDBY switch in the STDBY position and remove all test equipment.

5.7.8 Powerbase-to-Monitor Communication

AC power must be applied for this test.

1. Simultaneously press the TREND and EVENT buttons on the rear of the Powerbase.

2. Verify that the word "End" appears in the OXYGEN SATURATION display and the word "Prt" appears in the PULSE RATE display. This verifies Powerbase-to-Monitor Communication via the fiber optic link.

5.7.9 Monitor-to-Powerbase Communication

1. Locate the eight dip switches on the back of the Powerbase. Set switches 3 and 4 DOWN position and the rest in the UP position.

2. Verify that the FIBER OPTIC PORT labeled DATA on the rear of the Powerbase is not lighted.

3. Press the AUDIO ALARM OFF button on the front of the N-200 several times. Note that the FIBER OPTIC PORT labeled DATA lights up briefly each time the AUDIO ALARM OFF button is pressed.

5.7.10 Middle Daughter PCB Verification

1. Connect the DMM to the SAT connector on the rear of the Powerbase.

2. Locate the two dip switches on the rear of the Powerbase just above the SERIAL COMM port. Set the SaO_2 SCALE switch to the 0-100 position and the VOLT switch to the 0-10 position.

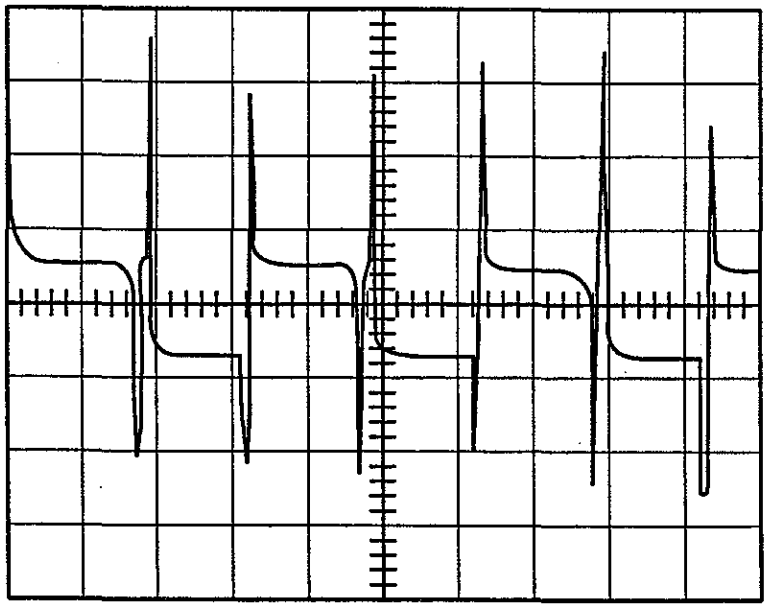
3. The DMM must read as follows depending on the indication of the OXYGEN SATURATION display.

OXYGEN SATURATION	DMM
80	8.00 ± 0.05 V
81	8.10 ± 0.05 V
82	8.20 ± 0.05 V

4. Repeat steps 2 and 3 with the SaO_2 switch set to the 50-100 position but use the values in the following table:

OXYGEN SATURATION	DMM
80	6.00 ± 0.05 V
81	6.20 ± 0.05 V
82	6.40 ± 0.05 V

5. Disconnect all test equipment and place the ON/STDBY switch to STDBY.



A

GAIN CH 1 0.2 V / div COUPLING AC TP −6

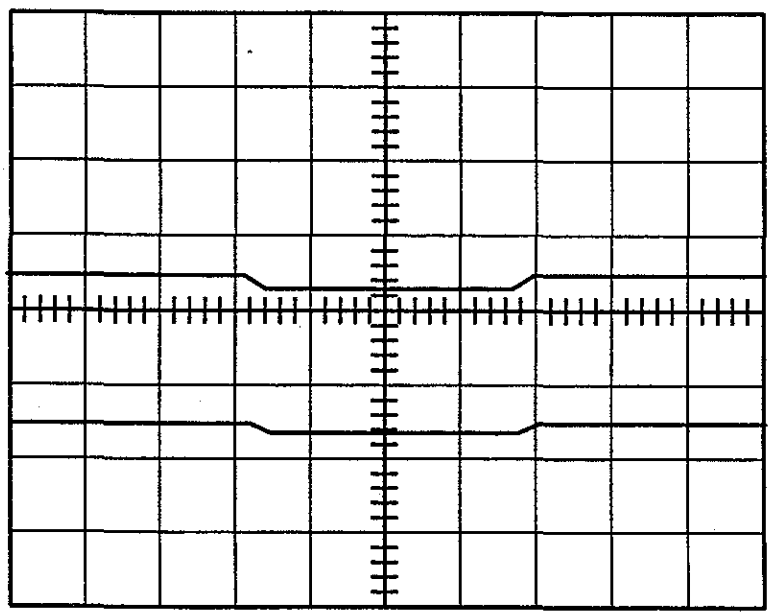
GAIN CH 2 not used COUPLING _____ TP _____

SWEEP SPEED 0.1 ms / div

SYNC _____

Channel 2

Channel 1



B

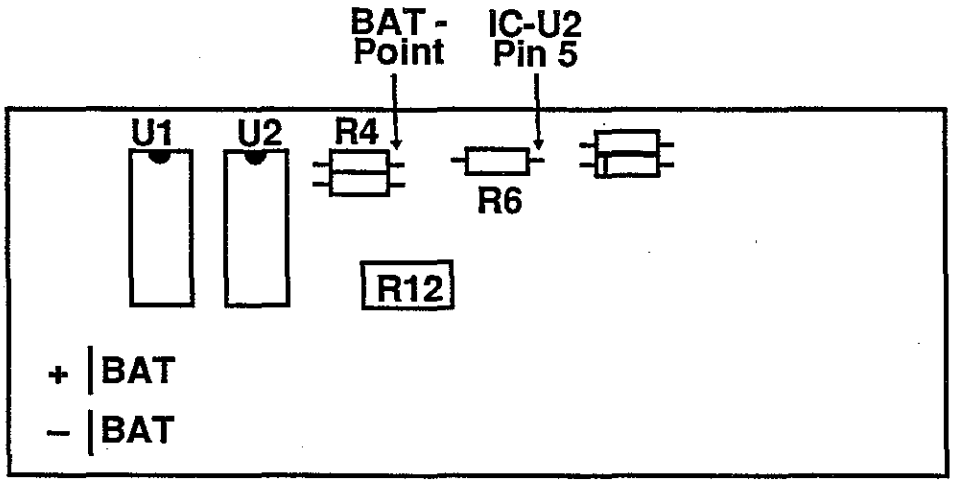
GAIN CH 1 2 V / div COUPLING DC TP −9

GAIN CH 2 2 V / div COUPLING DC TP −10

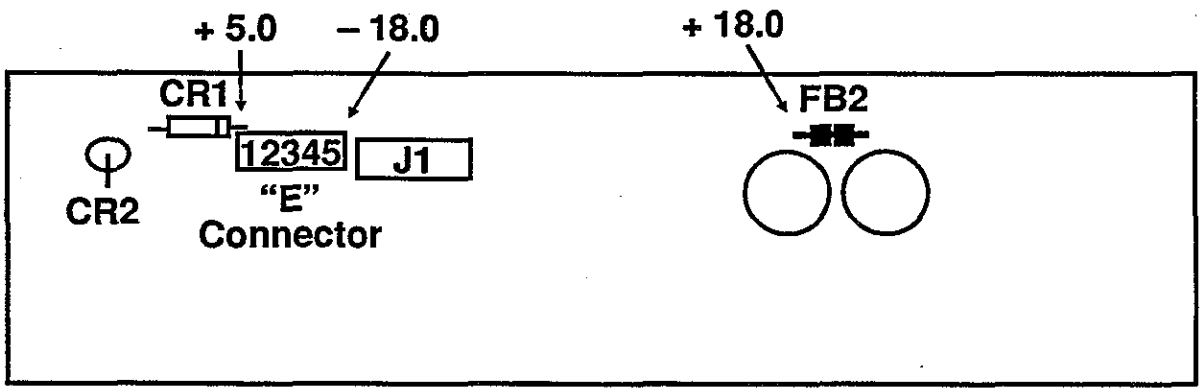
SWEEP SPEED 200 ms / div

SYNC _____

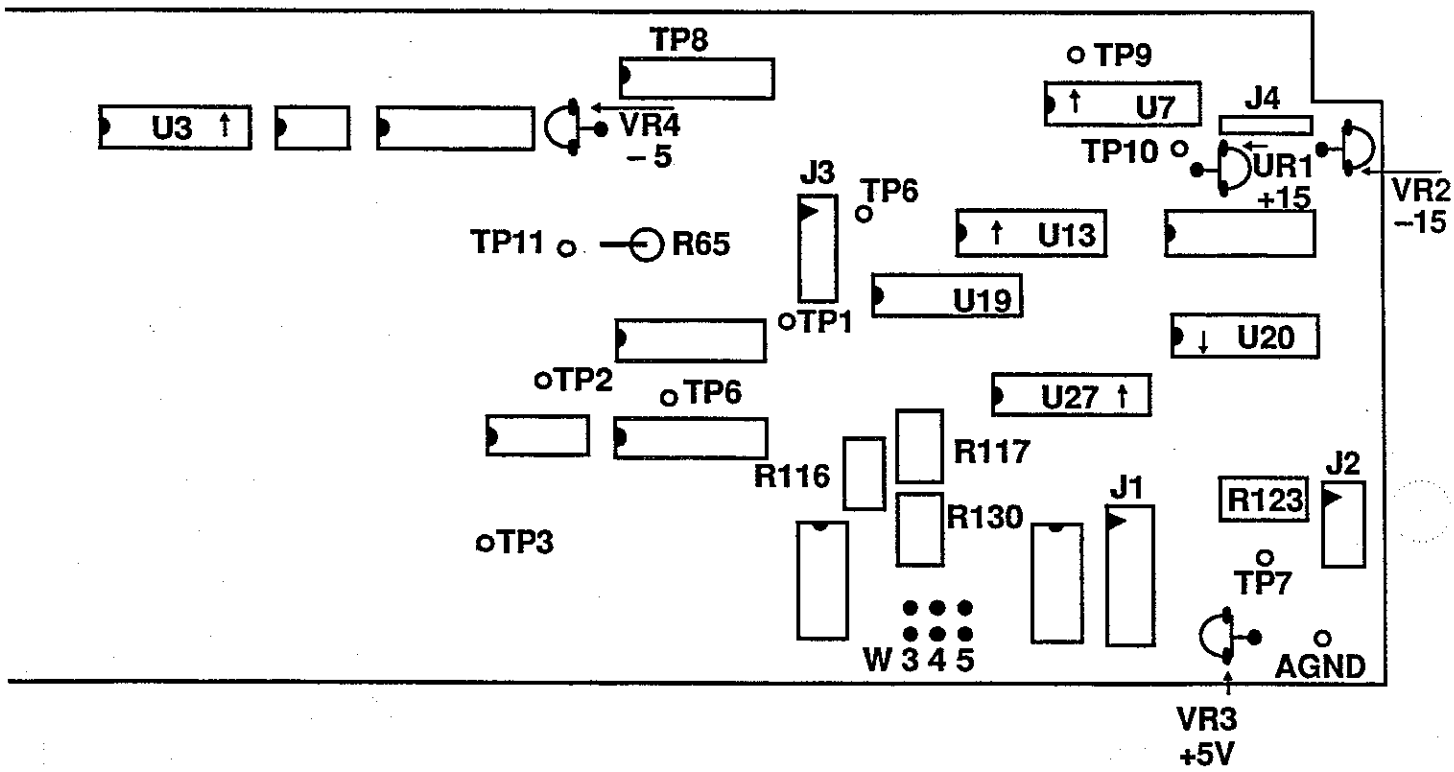
Attachment 1



N-200 Battery Charger Board Test Point Map



N-200 Power Supply Board



N-200 Processor Board Test Point Map

SECTION 7

PACKING FOR SHIPMENT

7.1. REPACKING IN ORIGINAL CARTON

The best package to use when packing the instrument for shipping is the original packing carton. If the original packing carton is available, pack the instrument as described in the following steps:

1. Snap the monitor and its powerbase together and place it in its plastic bag. The plastic bag is necessary to prevent abrading the instrument's front panel during shipment.

2. Place the instrument in the bottom piece of supporting foam, making sure that the ON/STNDBY switch on the bottom of the instrument fits into the recess made for it in the foam.

3. Place the upper foam pad on top of the instrument.

4. Place the instrument accessories (patient module, power cord, etc.) in the original accessories box and place the accessories box on top of the upper foam pad.

5. Securely seal the carton with packing tape.

7.2. PACKING IN DIFFERENT CARTON

If the instrument's original packing carton is not available, pack the instrument as described in the following steps:

1. Snap the monitor and its powerbase together and place it in a plastic bag.

2. Find a sturdy cardboard carton large enough to provide at least 2 inches of clearance on all sides of the instrument.

3. Fill the bottom of the carton with 2 inches of loose styrofoam packing material.

4. Place the instrument on the packing material and place the accessories on top of the instrument.

5. Fill the box completely with loose styrofoam packing material and securely seal the carton with packing tape.

SECTION 8

SPARE PARTS

8.1. EXTERNAL PARTS

Item*	Description	Part No.
—	ASSY, Power Cord	071505
—	Patient Module, 13'	072752
—	Patient Module, 20'	073145
1.4	Fuse, 1/2 Amp Slo-blow (100-120 V)	691011
1.5	Fuse, 1/4 Amp Slo-blow (220-240 V)	691098
1.6	Fuse, 4 Amp (Battery Pack)	691014

8.2. ELECTRICAL ASSEMBLIES

8.2.1. Monitor

Item*	Description	Part No.
2.1	ASSY, Power Supply PCB	072268
2.2	ASSY, Battery Charger PCB	072270
2.3	ASSY, Speaker	072487
2.4	ASSY, Processor PCB	072700
2.5	ASSY, Patient Cable	072756
2.6	ASSY, Encoder, Front Panel	072757
2.7	ASSY, Front Panel PCB Set	072758
2.8	ASSY, Battery Pack	073136
2.9	ASSY, On/Standby Switch	073217
2.10	Cable, Proc. PCB/Pwr. Sply PCB	053138
2.11	Cable, Processor PCB/Display PCB	053142

8.2.2. Powerbase

Item*	Description	Part No.
3.1	ASSY, Motherboard PCB	072120
3.2	ASSY, Upper Daughter PCB	072140
3.3	ASSY, Middle Daughter PCB	072150
3.4	ASSY, Lower Daughter PCB	072160
3.5	ASSY, AC Inlet/Transformer	073820

* Item numbers are keyed to the chassis-level assembly views in Section 8.4.

8.3. MECHANICAL PARTS

8.3.1 Monitor

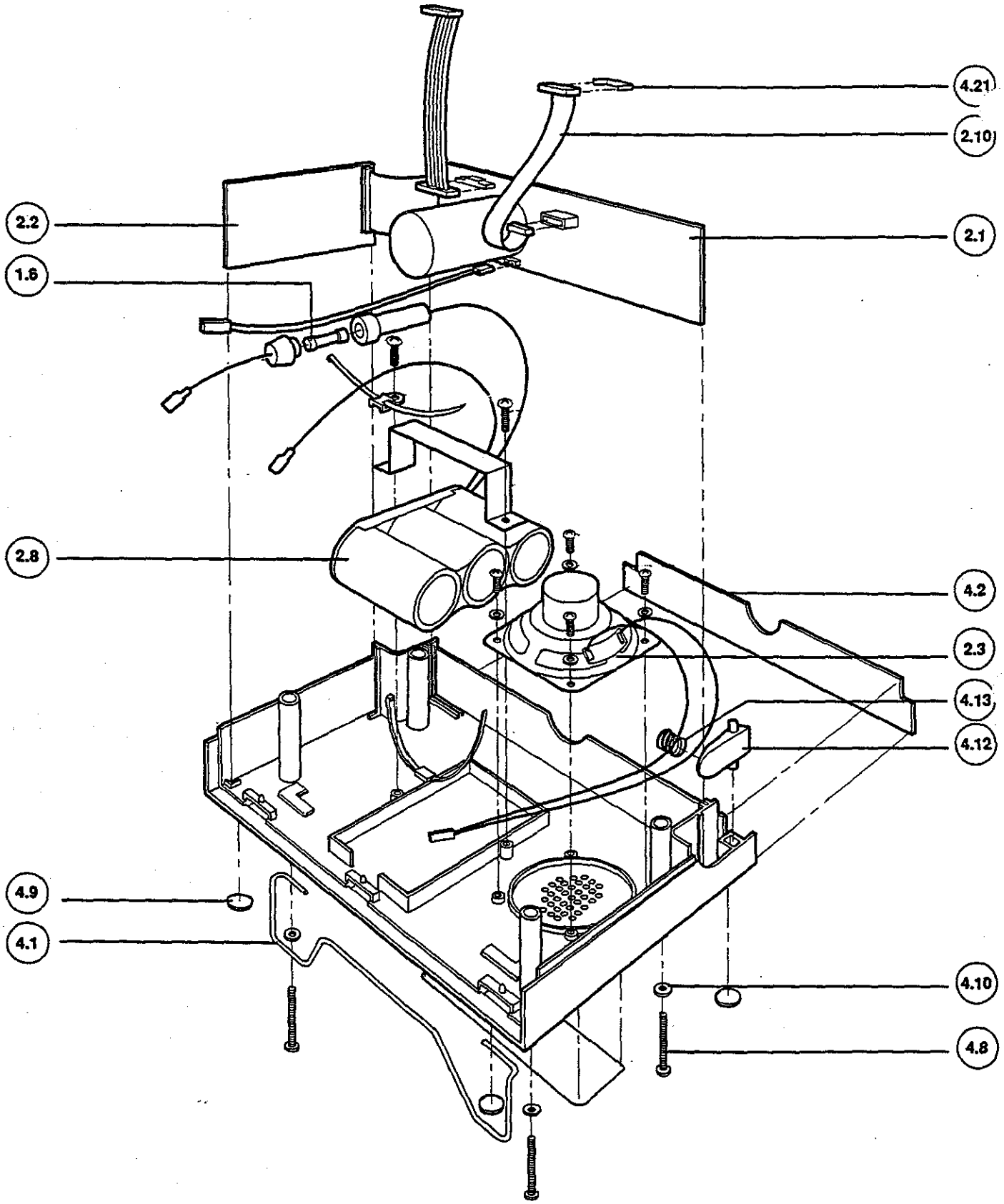
Item*	Description	Part No.
4.1	Wire Bail, Bottom Cover	052248
4.2	Gasket, Bottom Cover	052258
4.3	Gasket, Top Cover	053567
4.4	Keypad, Front Panel	052577
4.5	Top Cover	053724
4.6	Front Panel Window, Red	052719
4.7	Front Panel	053374
4.8	Screw, Top Cover	872063
4.9	Rubber Bumper, Bottom	759110
4.10	Washer, Top Cover	860202
4.11	Screw, Proc. PCB hold-down	871031
4.12	Latch	052262
4.13	Spring, Latch Compression	891064
4.14	Washer, Proc. PCB hold-down	891074
—	Patient Module Velcro Strap	052283
4.16	Knob, Front Panel	054235
4.17	Retaining Ring for Knob	891050
4.19	Clip, 20 Pin Connector	491100
4.20	Clip, 14 Pin Connector	491099
4.21	Clip, 10 Pin Connector	491098
4.22	Washer, LEMO Connector	491005
4.23	Nut, LEMO Connector	491006
4.24	Screw, Display Panel Assy.	871056

8.3.2 Powerbase

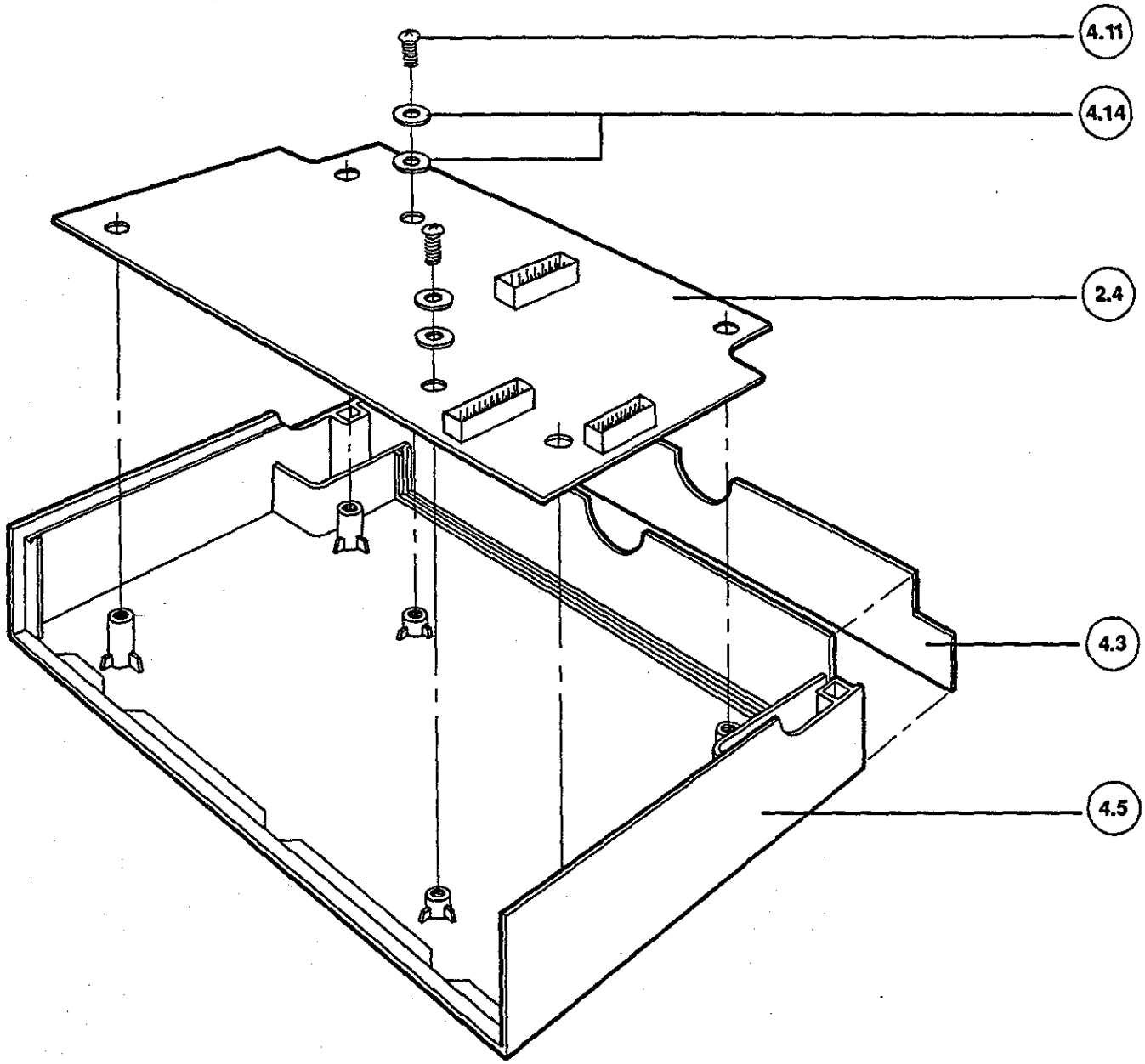
Item*	Description	Part No.
5.1	Top Cover	053897
5.2	Bottom Cover	052141
5.3	Backplate	052174
5.4	Pushbutton Cap	639101
5.5	Screw, Powerbase Covers	872163
5.6	Screw, Transformer Attachment	873100

* Item numbers are keyed to the chassis-level assembly views in Section 8.4.

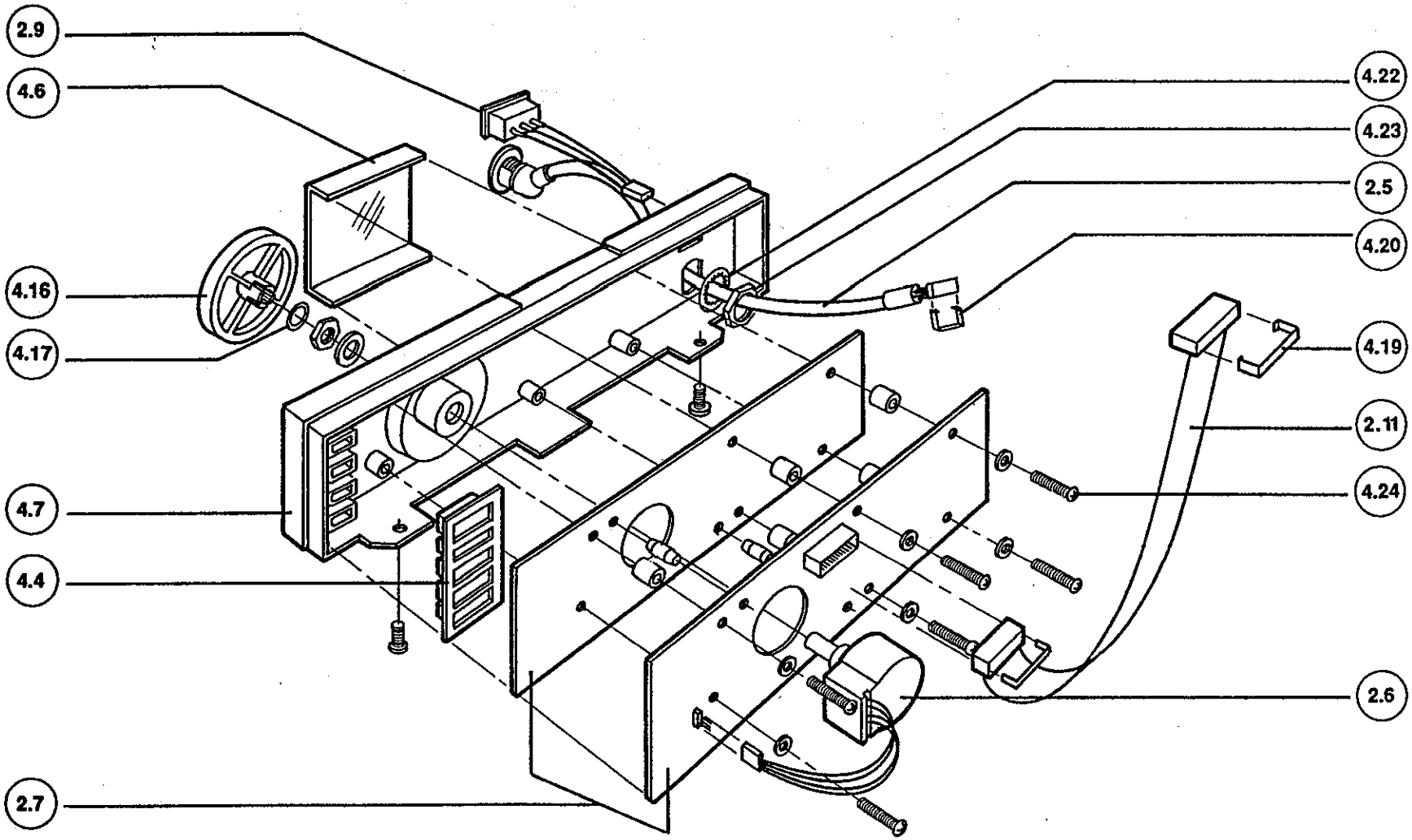
8.4. CHASSIS-LEVEL ASSEMBLY VIEWS



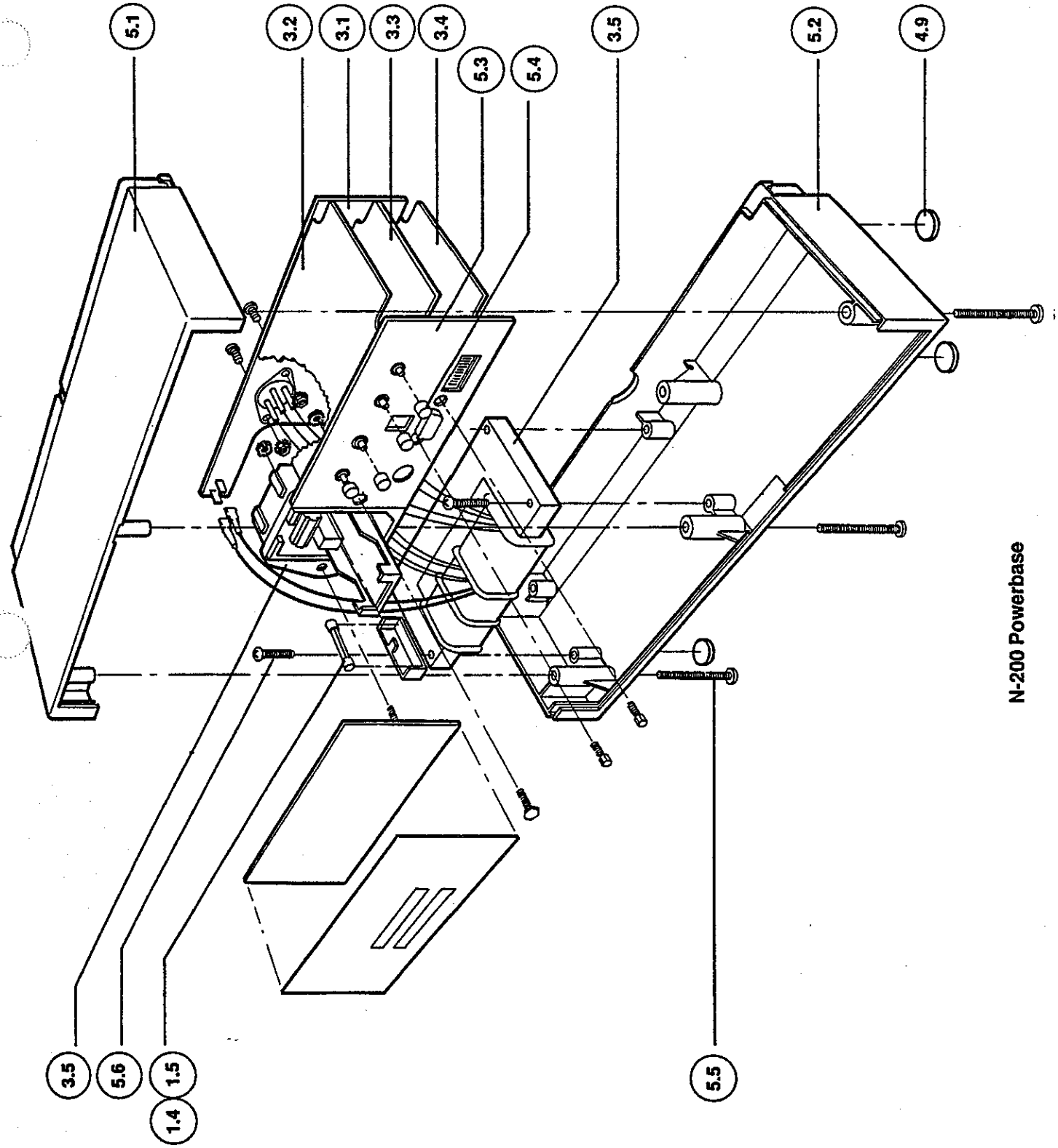
N-200 Monitor Chassis



N-200 Monitor Top Cover



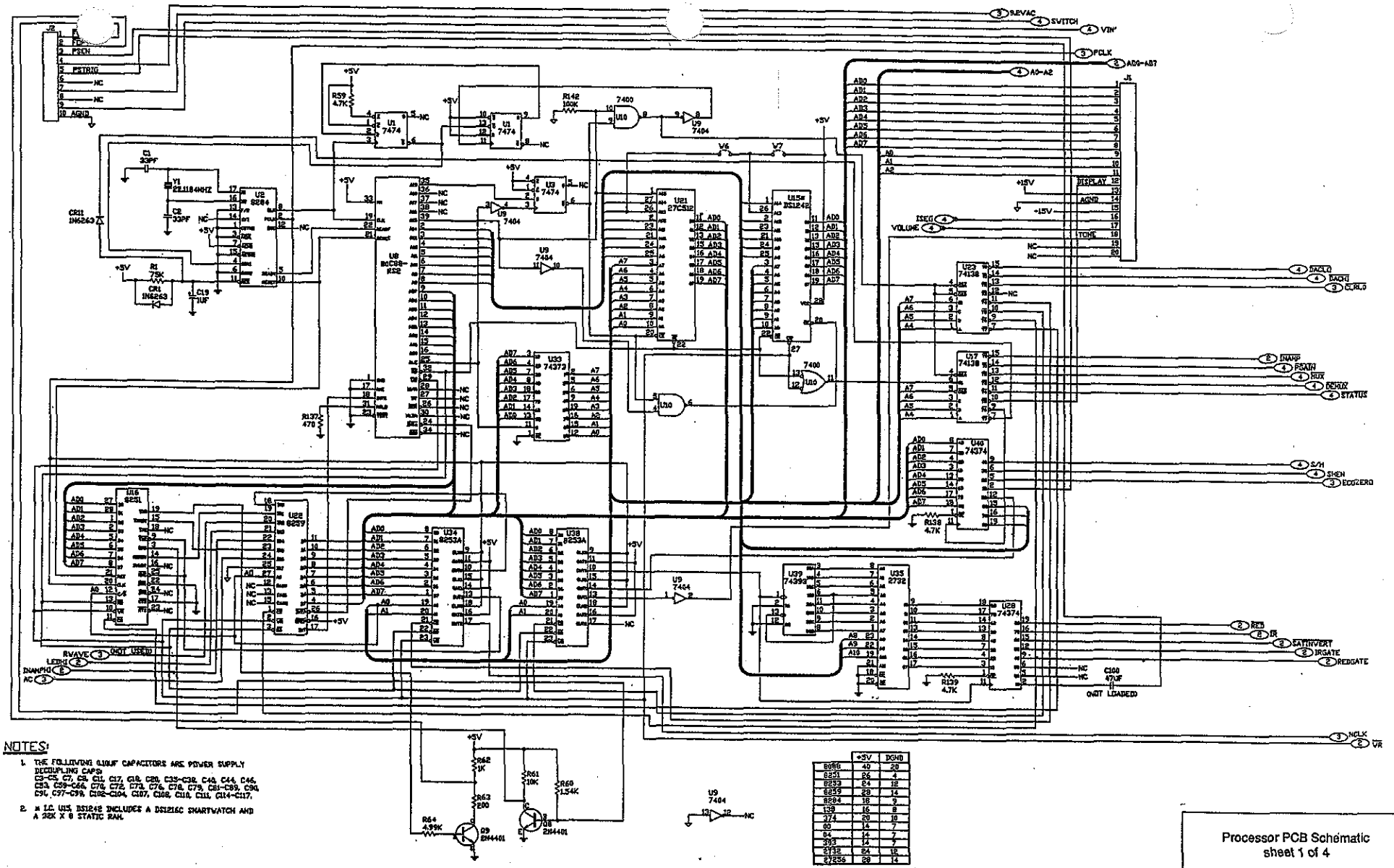
N-200 Monitor Front Panel

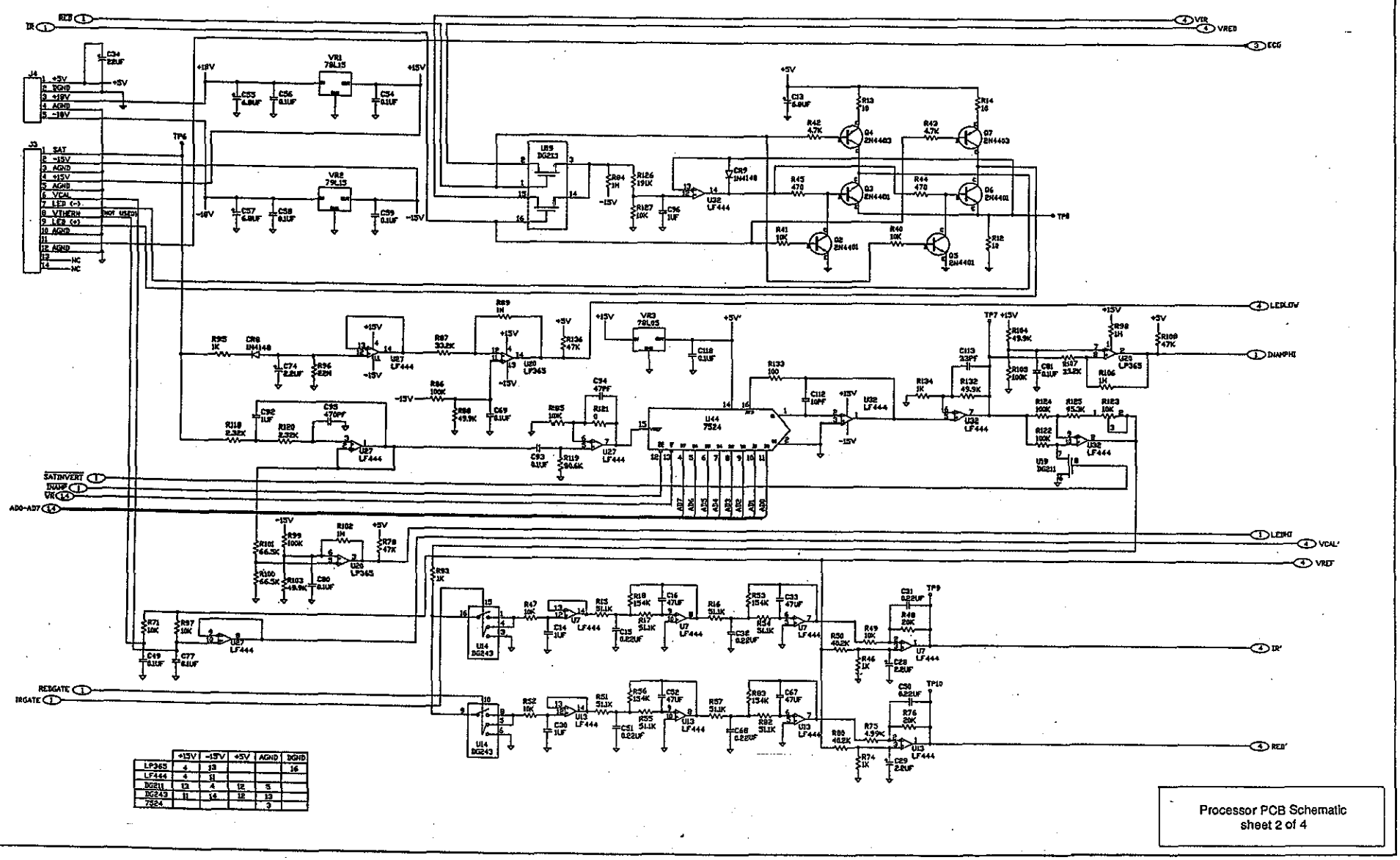


N-200 Powerbase

SECTION 9

SCHEMATIC DIAGRAMS


NOTES:
1. THE FOLLOWING 0.1UF CAPACITORS ARE POWER SUPPLY DECOUPLING CAPS:
C3-C5, C7, C8, C11, C17, C18, C20, C35-C38, C40, C44, C46, C53, C59-C64, C70, C72, C73, C76, C78, C79, C81-C89, C90, C91, C97-C99, C102-C104, C107, C108, C110, C111, C114-C117.
2. U LC. U15, DS1242 INCLUDES A DS1216C SMARTWATCH AND A 32K X 8 STATIC RAM.
Processor PCB Schematic
sheet 1 of 4



	+15V	-15V	+5V	AGND	DGND
LP365	4	13			16
LF444	4	11			
DG211	13	4	12	5	
DG243	11	14	12	13	
7524				3	

Processor PCB Schematic
sheet 2 of 4